Board Design Guidelines

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SECTION 1: INTRODUCTION

1.1 POLICY

These design guidelines, along with suitable materials, fabrications, and assembly processes can be applied by engineers and designers to achieve consistently manufacturable, high quality, reliable printed wiring boards and assemblies.

It is the responsibility of the CAD design group to maintain this document. Representatives of all groups involved in the design and manufacturing of the printed wiring boards and assemblies will have the responsibility of reviewing this document for accuracy and usefulness.

1.2 PURPOSE

This document is intended to be used as a guide in the engineering and layout of printed wiring boards and assemblies. Guidelines are presented to aid in the design of manufacturable and reliable printed wiring assemblies. PCB fabrication and assembly processes in common use are described along with the advantages and limitations concerning their application. Preferred processes and design practices are recommended to optimize the fabrication and assembly processes, as well as identify manufacturing limitations. It is not possible to exhaustively describe the full capability of Altron Inc.'s assembly processes; therefore, electrical and manufacturing engineering should be consulted when processes or design requirements not presented in this document are required.

1.3 SCOPE

The guidelines and requirements in this document apply to the design and manufacture of printed wiring boards and assemblies. If possible, pad geometry and outer layers should be reviewed by qualified assembly personnel for potential problems. Proper pad design will allow the desired I-R, vapor phase, convection, or wave solder results.

(NOTE: ALL DIMENSIONS IN THIS MANUAL ARE EXPRESSED IN INCHES)

SECTION 2: GENERAL DESIGN STANDARDS

The following sections contain design standards common to printed wiring boards. In the case of small and flex type boards, where exceptions to these standards may be required, fabrication and assembly vendors should be consulted and approval sought from the responsible engineering group.

2.1 CIRCUIT LAYERS

All circuit layers, including power and ground layers, will contain the layer number etched in copper. The numbers will be staggered in such a way that all numbers, except for the bottom layer number, will be in order and readable when looking through the top of the board (see Figure 2-1). The bottom layer number will be readable from the bottom of the board.

Figure 2-1 PLACING LAYER NUMBERS ON THE BOARD

2.2 SILKSCREEN AND COMPONENT ID

An attempt should be made to provide designators for all component outlines shown on the silkscreen. Designators should be readable when components are installed.

Indicate pin 1 on all connectors, headers, crystals, and any other component where pin 1 is not readily identifiable.

2.3 PANELIZATION AND TAB ROUTING

Panelization is the placing of 2 or more board images on blank material for processing, thus saving time and material over processing one board at a time (see Figure 2-2). A series of holes are drilled at several locations along the edge of the board, and the board outline is partially routed to form a tab to hold the processed board in the blank. The board may then be snapped out of the blank before or after components have been installed and soldered. Consult manufacturing engineering to determine if panelization is required and for the correct panel/board layout.

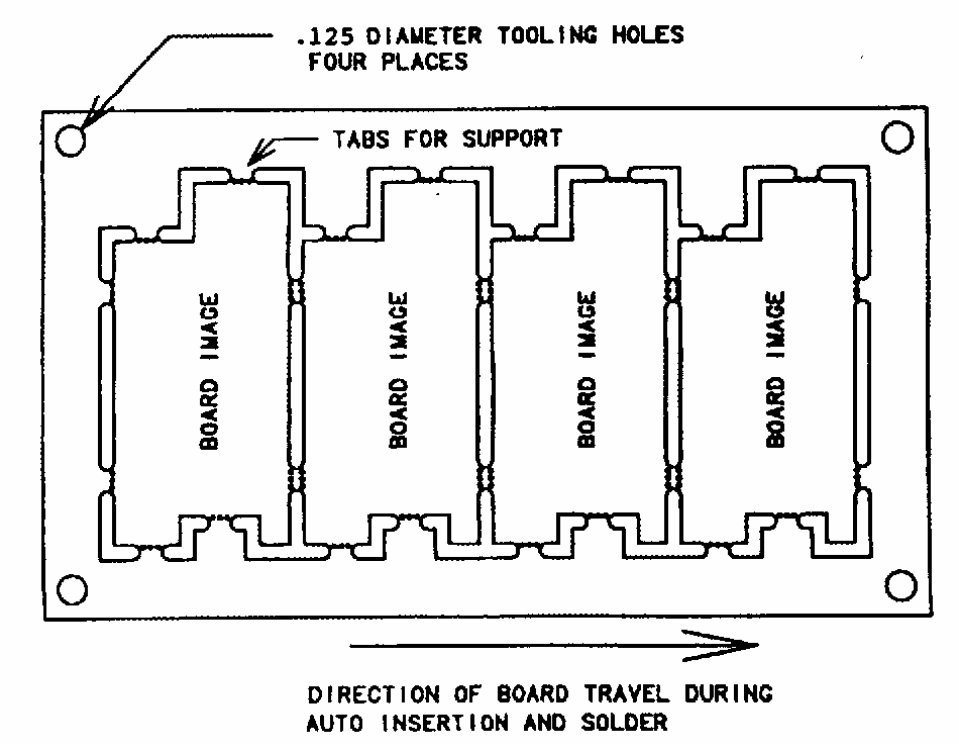


Figure 2-2 AN EXAMPLE OF PANELIZATION

At times, an irregularly shaped PWB may need tab routing to maintain a rectangular shape for board support in later processes such as auto insertion and soldering (see Figure 2-3). The extra board material may then be snapped off after the assembly is complete. Be aware that tab locations may interfere with installation of the board into later assemblies, and the appropriate engineering groups should be consulted to determine correct tab placement and board configuration.

An example of a tab would be 5 holes with center to center spacing of 0.041" and a hole diameter of 0.021".

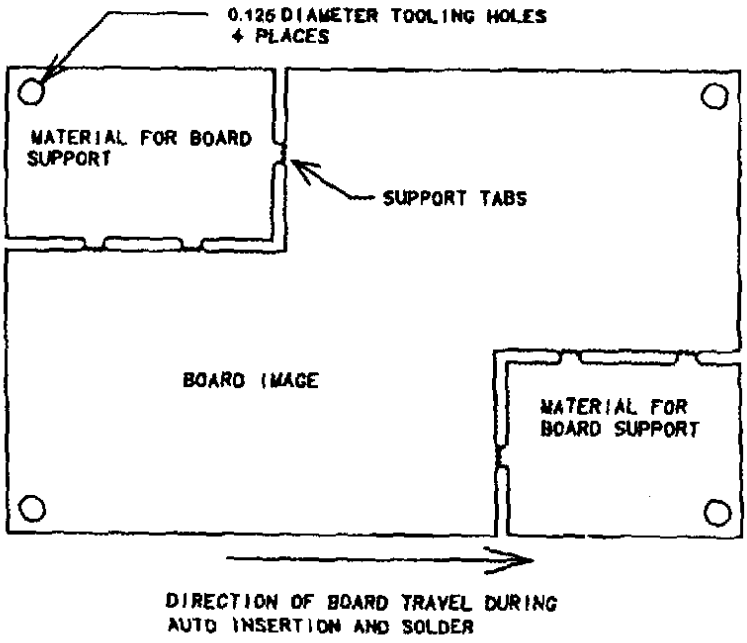


Figure 2-3 SUPPORTING AN IRREGULAR BOARD WITH TAB ROUTING

2.4 SOLDER MASK

** PAD CAP OUTER LAYERS ARE RECOMMENDED **

If used, solder mask clearance is required around all surface mount and through hole pads, tooling holes, shield contact areas, fiducials, and any areas where electrical contact or soldering is required. Check board fabricator for guidelines.

2.5 TOOLING HOLES

Tooling holes are required for positioning the PWB in machines and fixtures needed to process the board (e.g. drill machines, routing fixtures, auto insertion equipment and test fixtures). The configuration of the holes must be (4) 0.125" + 0.002" / -0.000" diameter holes, unplated, in each corner of the board and 0.200" from the edges. A component free area of approximately 0.400" from the center of the hole must be maintained because of tooling contact with the board and limitations on auto placement insertion heads (see Figure 2-3). These requirements may vary for insertion machines, therefore tooling holes and restricted areas should be verified.

SECTION 3: SMT PAD GEOMETRIES

3.1 GENERAL GUIDELINES

When designing pads for components not specifically covered in this manual, it is suggested that manufacturing, part vendors and assembly vendors be contacted for design recommendations.

The nominal dimensions of components will be used to design pad geometries.

Whenever possible, measure the physical component and design the pad to those dimensions. Caution is advised when designing for a component with multiple vendors as package dimensions may not be the same. It is possible to design a common pad for multiple parts providing the dimensions do not vary too greatly. It is not recommended to design pads more than 0.010" larger than the normal pad design for a given part. The nominal pad design shall be recommendations from part or assembly vendors, or pads derived from this design document. Do not design pads smaller than nominal.

Some parts are not compatible with the wave solder process and should not be designed for use on the solder side of assemblies as damage to the components may occur during soldering. Refer to Section 5.9 for components not recommended for solder side usage.

3.2 PAD AND COMPONENT TERMINOLOGY

The following terms will apply for surface mount components and pad geometries (see Figure 3).

TERMINATION: The metallization band on the end of a chip component.

TERMINATION WIDTH: The dimension of the termination across the component. On some components the termination may not extend across the total width of the part. Various tantalum caps are an example of this type of termination (see Figure 3-5).

EXTENSION: The length of exposed pad area where the solder fillet forms during solder.

OVERLAP: The area of pad covered by the component termination. The length of the overlap will normally include a tolerance for misalignment.

TOLERANCE: The amount of pad added under the component for misalignment.

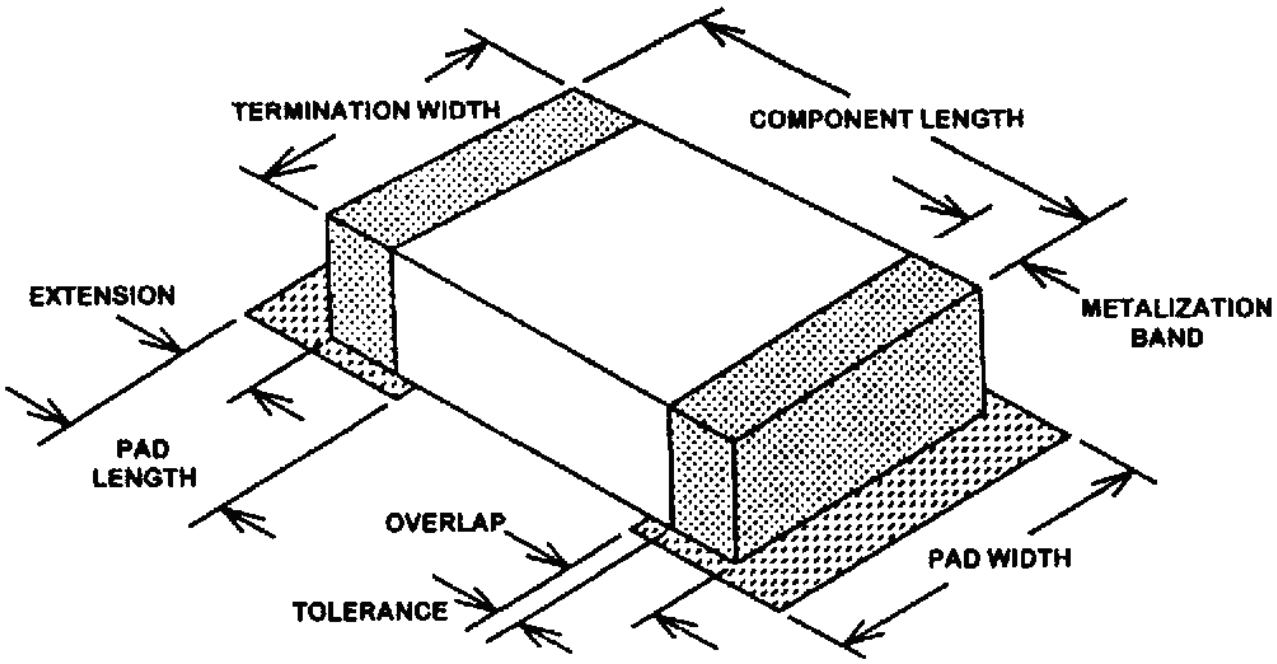


Figure 3 PAD TERMINOLOGY

3.3 REFLOW PADS FOR 0201 CHIPS

The reflow pad width will be equal to the component termination width + 0.005" (see Figure 3-1).

The reflow pad length will be the dimension of the termination band plus a 0.010" extension plus a 0.001" overlap (see Figure 3-1).

The pad to pad spacing will be the component length minus 2X the termination band dimension minus 0.002" overlap.

FOR EXAMPLE, a component with a 0.020" body length, 0.010" termination width, and 0.005" termination band, will need a pad 0.016" long, 0.015" wide, and a pad spacing of 0.008".

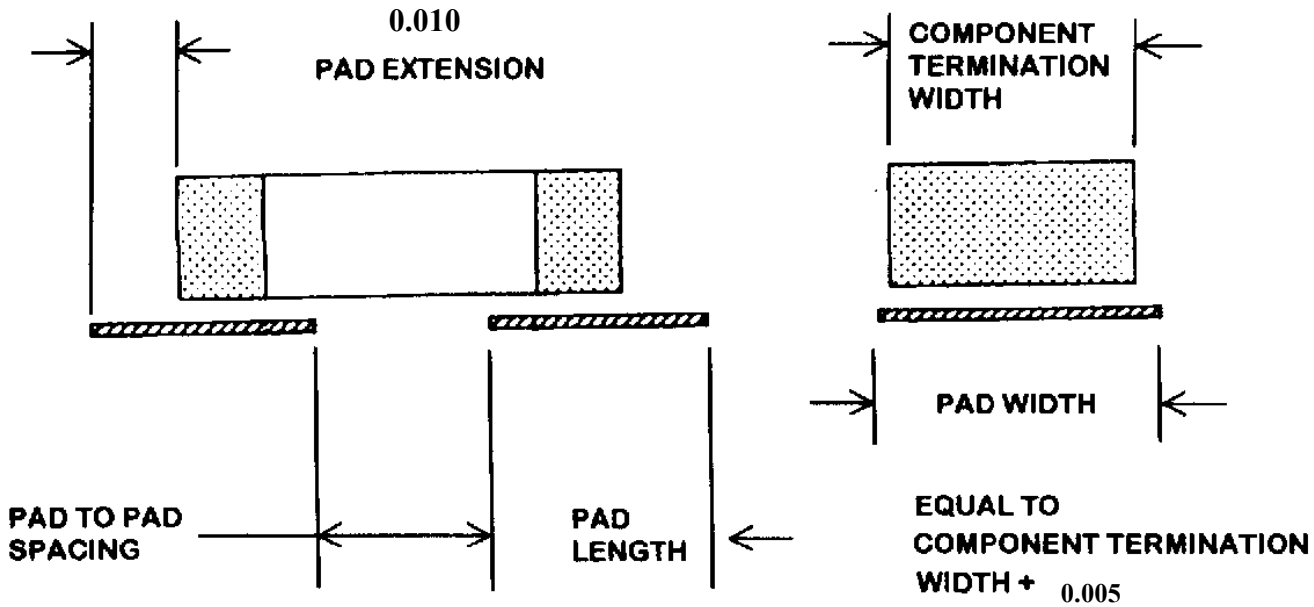


Figure 3-1 SOLDER PADS FOR 0201 CHIP COMPONENTS

3.4 REFLOW PADS FOR 0402 CHIPS

The reflow pad width will be equal to the component termination width + 0.010" (see Figure 3-2).

The reflow pad length will be the dimension of the termination band plus a 0.015" extension plus a 0.002" overlap (see Figure 3-2).

The pad to pad spacing will be the component length minus 2X the termination band dimension minus 0.004" of overlap.

FOR EXAMPLE, a component with a 0.040" body length, 0.020" termination width, and 0.010" termination band, will need a pad 0.027" long, 0.030" wide, and a pad spacing of 0.016".

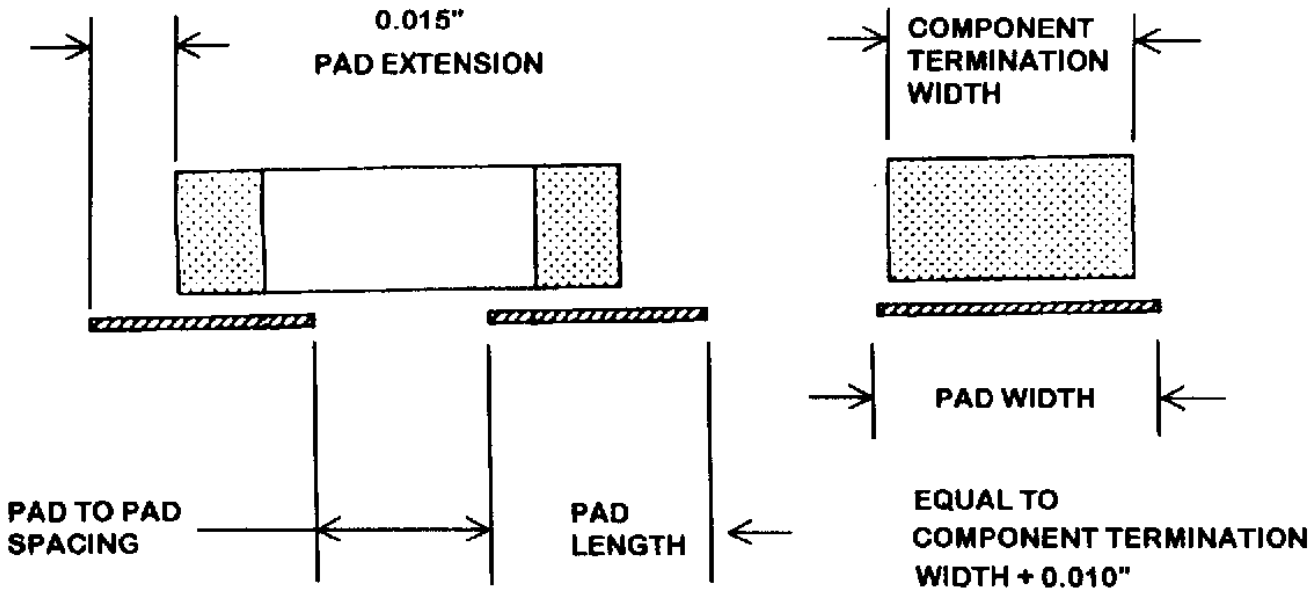


Figure 3-2 SOLDER PADS FOR 0402 CHIP COMPONENTS

3.5 REFLOW PADS FOR 0603 AND 0805 CHIPS

The reflow pad width will be equal to the component termination width + 0.010" (see Figure 3-3).

The reflow pad length will be the dimension of the termination band plus a 0.020" extension plus a 0.002" overlap (see Figure 3-3).

The pad to pad spacing will be the component length minus 2X the termination band dimension minus 0.004" of overlap.

FOR EXAMPLE, a component with a 0.080" body length, 0.050" termination width, and 0.015" termination band, will need a pad 0.037" long, 0.060" wide, and a pad spacing of 0.046".

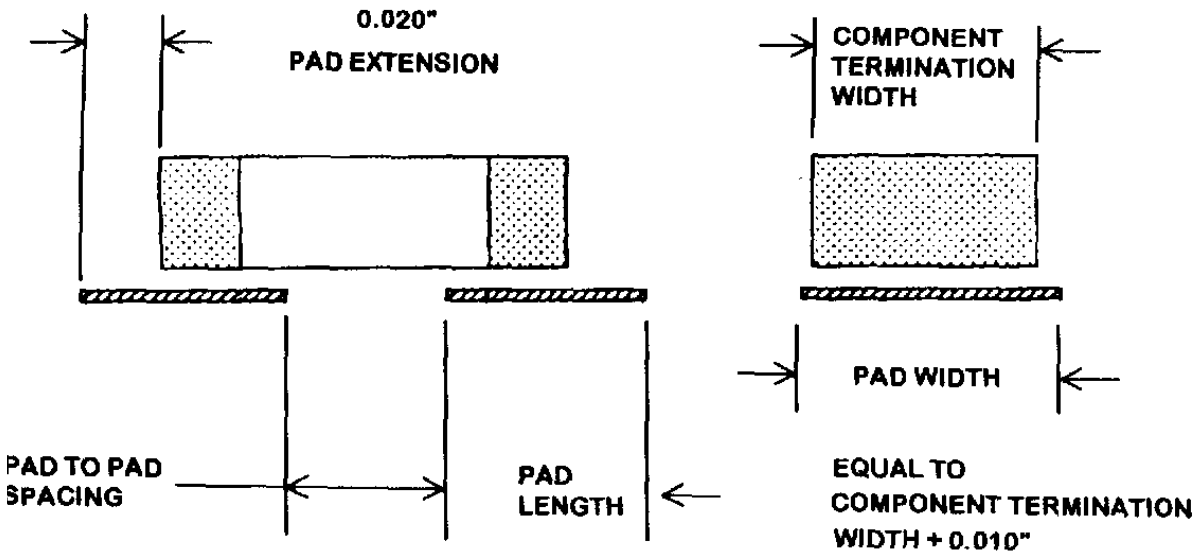


Figure 3-3 SOLDER PADS FOR 0603 AND 0805 CHIP COMPONENTS

3.6 REFLOW SOLDER PADS FOR 1206 CHIPS

The reflow pad width will be equal to the component termination width + 0.010" (see Figure 3-4).

The reflow pad length will be the dimension of the termination band plus a 0.025" extension plus a 0.002" overlap (see Figure 3-4).

The pad to pad spacing will be the component length minus 2X the termination band dimension minus 0.004" of overlap.

FOR EXAMPLE, a component with a 0.120" body length, 0.060" termination width, and 0.020" termination band, will need a pad 0.047" long, 0.070" wide, and a pad spacing of 0.076".

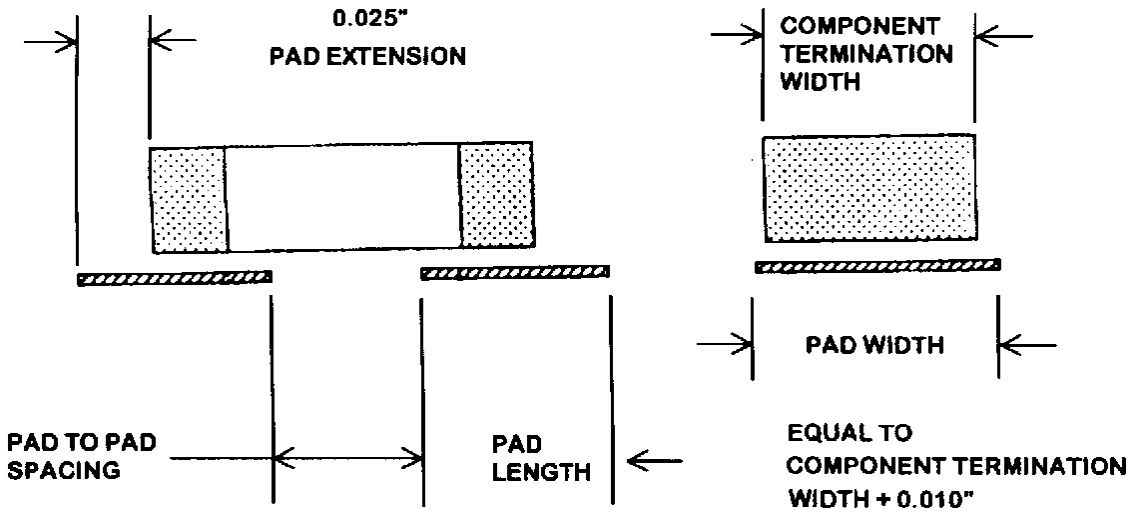


Figure 3-4 SOLDER PADS FOR CHIP COMPONENTS

3.7 REFLOW PADS FOR TANTALUM CAPACITORS

The reflow pad width will be equal to the component termination width + 0.010" (see Figure 3-5).

The reflow pad length will be the dimension of the termination area or leg plus a 0.025" extension and a 0.002" overlap (see Figure 3-5).

The pad to pad spacing will be the component length minus 2X the termination leg dimension minus 0.004" of overlap.

FOR EXAMPLE, a component with a 0.235" body length and termination length and width of 0.035" X 0.085", will need a pad 0.062" long, 0.095" wide, and a pad spacing of 0.161".

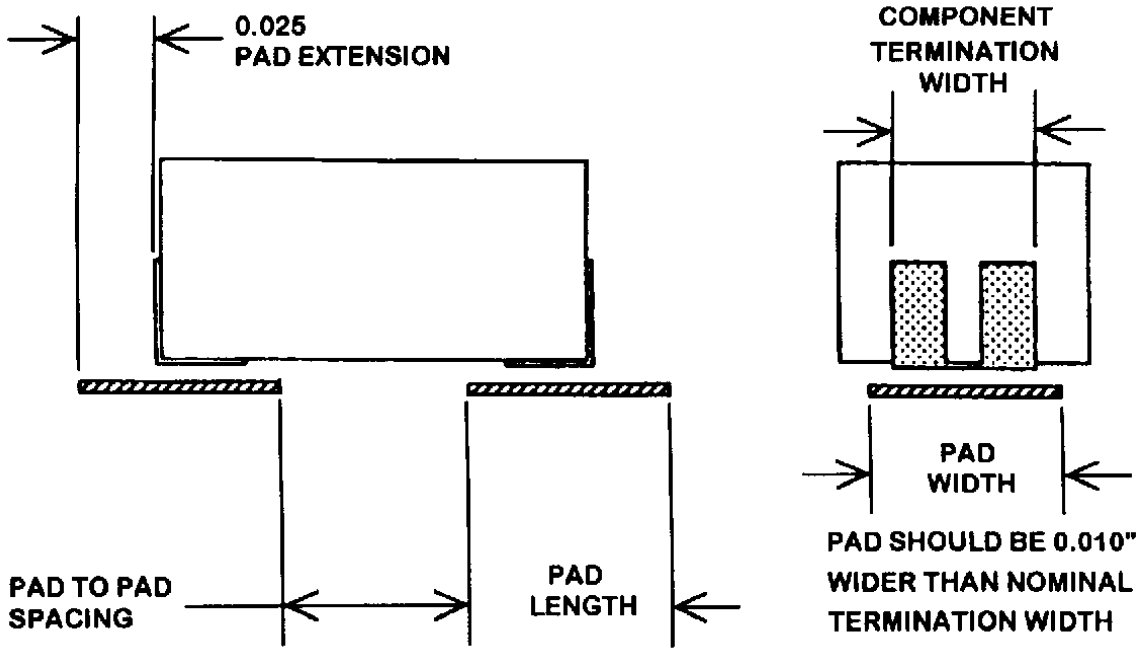


Figure 3-5 PADS FOR TANTALUM CAPACITORS

3.8 REFLOW PADS FOR SOIC

The reflow pad width will be ½ the lead pitch.

The reflow pad length to be twice the lead foot length.

The pad to pad spacing shall be ½ the lead pitch.

Using the nominal dimensions of the component heel and toe extensions of 0.010" - 0.020" (0.010" minimum) is required on the inside and outside of the pad for formation of the solder fillet. A larger heel may cause an excess solder condition on the inside of the lead reducing flexibility and increasing stresses on the solder joint (see Figure 3-6).

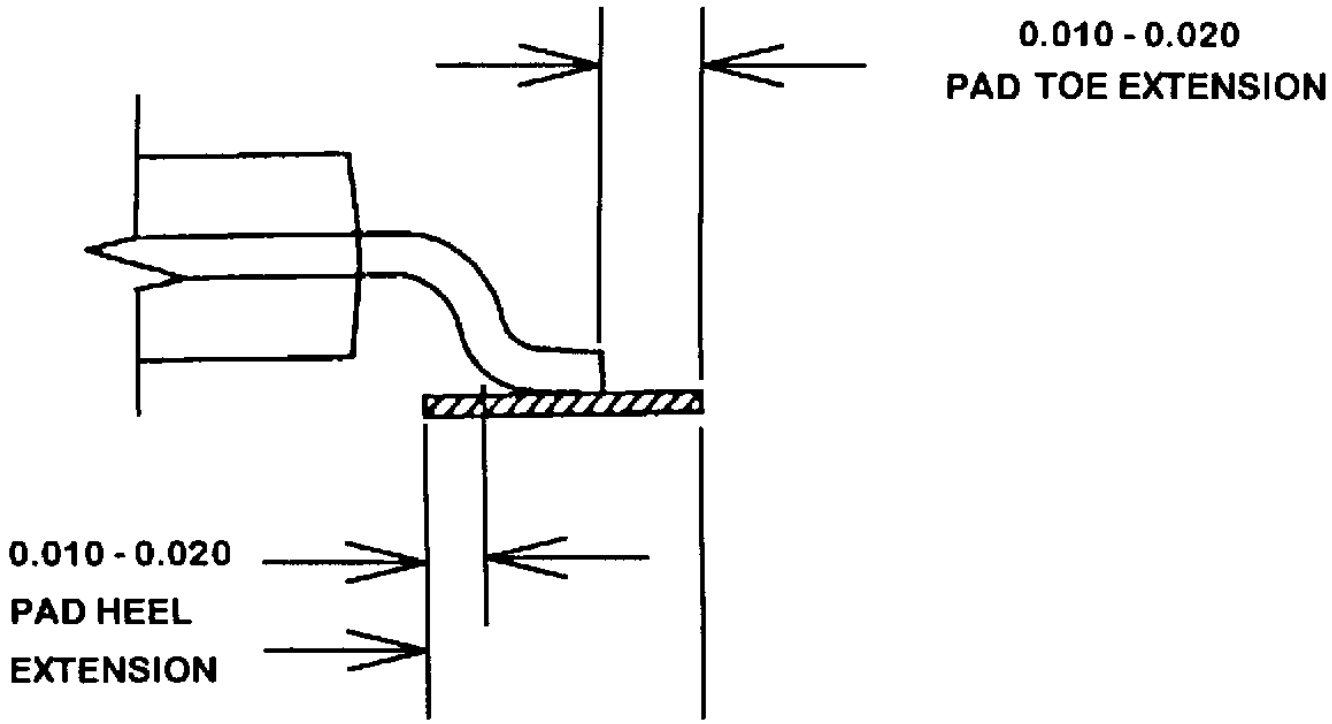


Figure 3-6 SOIC PADS

3.9 REFLOW PADS FOR PLCC

The reflow pad width will be 1/2 the lead pitch. A pad 0.025" wide is recommended for 0.050” lead pitch.

The reflow pad length to be the nominal dimension of component lead + 0.010" - 0.020". A smaller extension may experience shadowing problems. Larger extensions have no advantage (see Figure 3-7).

The pad to pad spacing to be ½ the lead pitch.

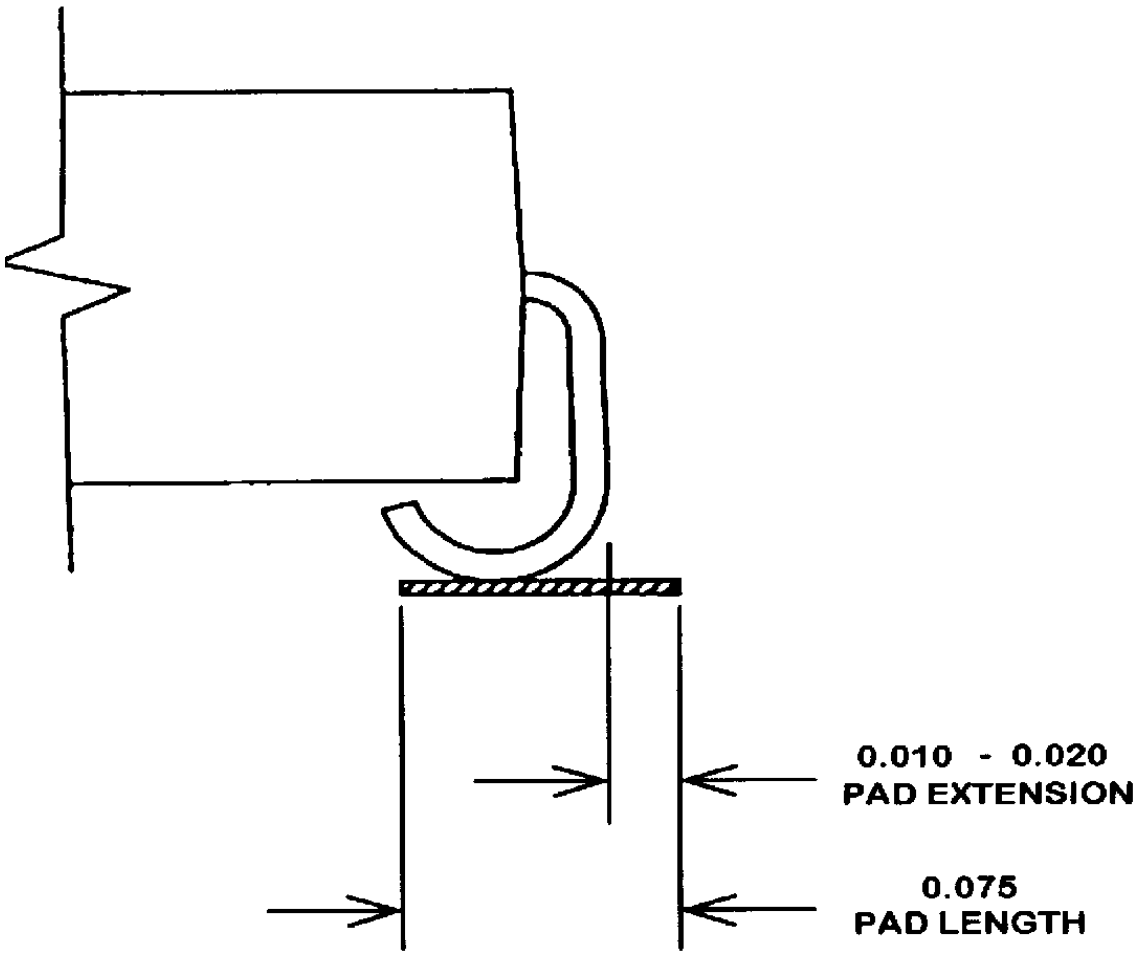


Figure 3-7 PLCC PADS

3.10 REFLOW PADS FOR MELF

The reflow pad width will be 0.010" wider than the component diameter (see Figure 3-8).

The reflow pad length will be the dimension of the termination band plus a 0.025" extension plus a 0.002" overlap (see Figure 3-8).

The pad to pad spacing will be the component length minus 2X the termination band dimension minus 0.004" of overlap.

FOR EXAMPLE, a component with a 0.140" body length, 0.015" termination length and 0.065" diameter, must have a pad 0.042" long, 0.075" wide, and a pad spacing of 0.106".

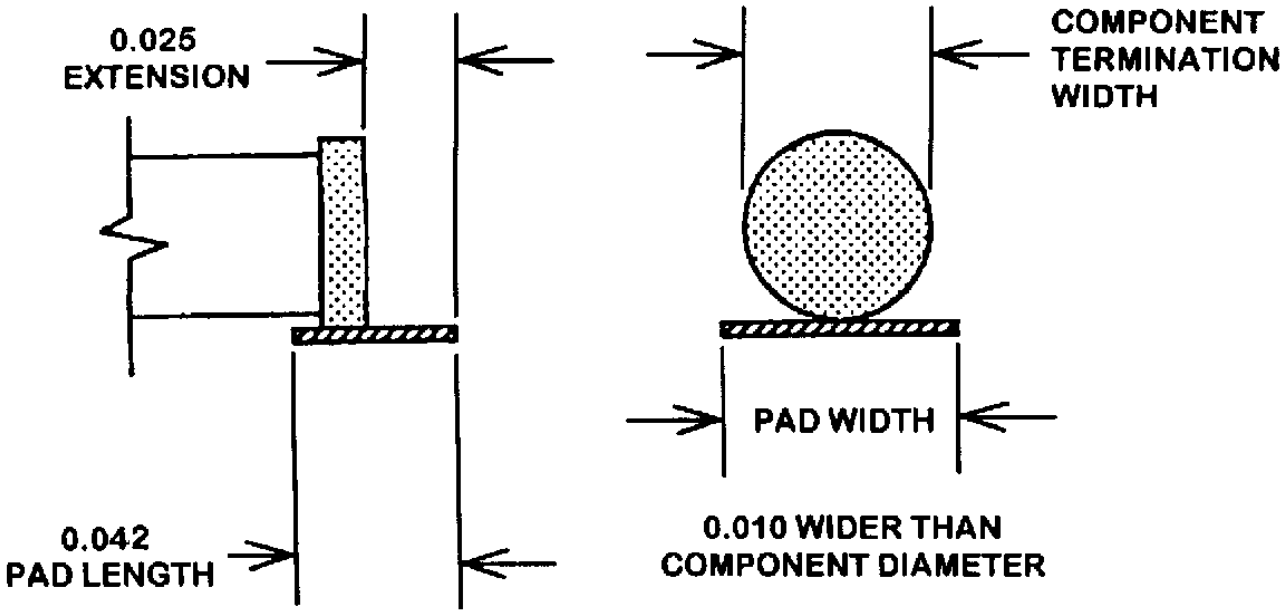


Figure 3-8 MELF PADS

3.11 REFLOW PADS FOR BGA

There are two types of pads: Non Solder Mask Defined Pad (NSMD) and Solder Mask Defined Pad (SMD)). The advantage of the NSMD pad is that the pad is smaller than that of an SMD pad. This allows more room for traces. This may be especially important when using micro BGAs.

Figure 3-9 shows an example of a Ball Grid Array (BGA) pad design. When the pads of a BGA are designed, the type of BGA must be taken into account. Since Plastic Ball Grid Arrays (PBGA) use Sn63 solder balls and Ceramic Ball Grid Arrays (CBGA) use Sn10, they each require a specific pad design. Table 3-1 gives an example of the dimensions of a l.27mm PBGA and a 1 .27mm CBGA.

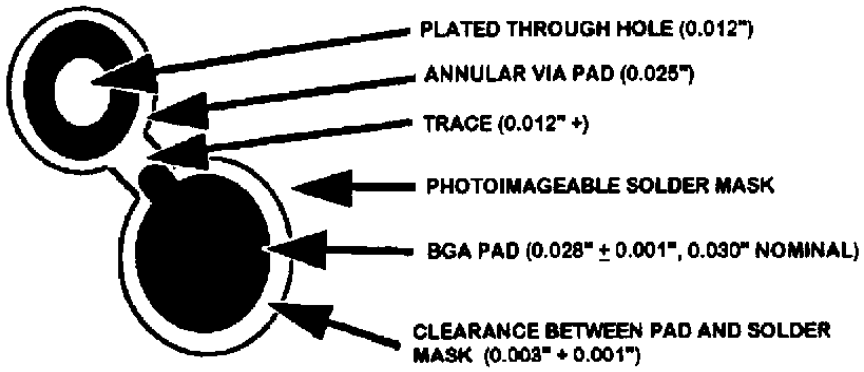


Figure 3-9 EXAMPLE OF 1.27MM CBGA NSMD PAD

	PLASTIC BGA		CERAMIC BGA	
PAD TYPE	SMD	NSMD	SMD	NSMD
VIA DIA.	0.012"	0.012"	0.012"	0.012"
PAD DIA.	0.025"	0.025"	0.025"	0.025"
SOLDER PAD DIA.	0.031"	0.023"	0.033"	0.0285" ± 0.0015"
MASK CLEARANCE	N/A	0.003" ± 0.001"	N/A	0.003" ± 0.001"

Table 3-1 EXAMPLE OF 1.27MM CBGA AND PBGA

SECTION 4: CREATING CAD PARTS

4.1 COMPONENT OUTLINES AND REFERENCE DESIGNATORS

The component silkscreen outlines should reflect the maximum case size of the component to aid in correct placement. The component outline will use a line width of 0.010". Silkscreen must be kept away from the pad area.

Outlines or reference designators should not be located under the component body to avoid raising the part above the pads, or creating a pivot point which can lead to tombstoning.

SECTION 5: COMPONENT PLACEMENT AND ORIENTATION

5.1 GENERAL ENGINEERING REQUIREMENTS

THESE REQUIREMENTS ALSO APPLY TO THROUGH HOLE COMPONENTS

Components should be arranged in rows and columns, and oriented uniformly for ease of installation, inspection and repair. They should also be located in a manner which best answers the criteria of the circuit.

Provide a clear area of 0.125" (minimum) on the top and bottom sides of the PWB for clearance of card guides, tooling for wave solder and wave solder stiffeners.

Orient all polarized components such as caps and diodes in the same direction. Polarity of all polarized components must be indicated on the silkscreen.

Locate test points, switches, jumpers and adjustable components for easy access during test.

Place components to achieve a clean separation between analog and digital grounds and voltages.

Separate inputs from outputs as much as possible.

Locate high heat or heat sensitive components so that thermal actions are minimized.

5.2 GENERAL PLACEMENT GUIDELINES

Orient like components in the same direction and the correct orientation for efficient placement and soldering. (See Section 5.7 for correct component orientation for soldering.)

Components placed on the solder side of the board directly behind a large number of PTH leads should be avoided. Avoid designs which surround solder side SMT components on all sides with PTH leads. Trapped gasses may block solder and the PTH leads disrupt solder flow to the SMD terminations. An example of this is chip capacitors directly under through hole sockets for PGA's, PLCC and LCC packages.

When possible, place all SMT components on the same side of the board and all through hole components on the component side (top). This keeps the number of processes required to solder an assembly to a minimum. When an assembly contains SMT components top and bottom and through hole components on top, the assembly requires an extra epoxy process to solder the bottom side SMT components. PLCC packages are not to be placed on the solder side of the board on mixed technology boards.

5.3 FIDUCIALS

As an aid to automatic placement, three global fiducial marks are required on the board surfaces which contain surface mount components. An area (0.125 inch radius) around the fiducial mark is to be free of all silkscreen, solder mask, traces, pads and text. Fiducial marks must be located within an area as outlined in Figure 5-1. As an aid in placing fine pitch components (less than 0.030" pitch), a fiducial mark should be located on the surface of the board at tile center of the part in addition to using two global fiducial marks.

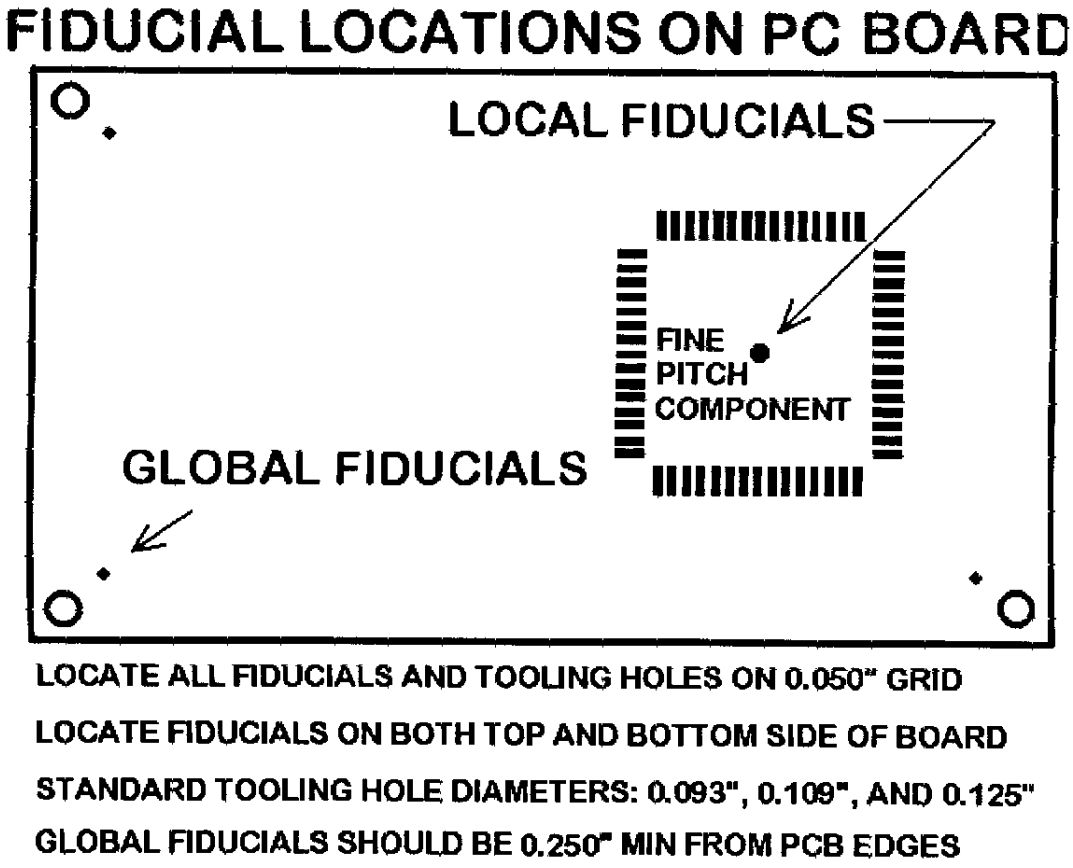


Figure 5-1 FIDUCIAL LOCATIONS

5.4 COMPONENT SPACING

Component to component spacing is critical to soldering, rework, test and automated assembly. If components are placed too close together, the placement head of pick and place machines may interfere with other components requiring manual placement of some parts. Also, any of these conditions may cause a longer more costly assembly process and less reliable product.

When placing chip components on the bottom of a board in a staggered pattern, a minimum spacing of 0.100" is required to insure that shadowing and unsoldered terminations do not occur (see Figure 5-2).

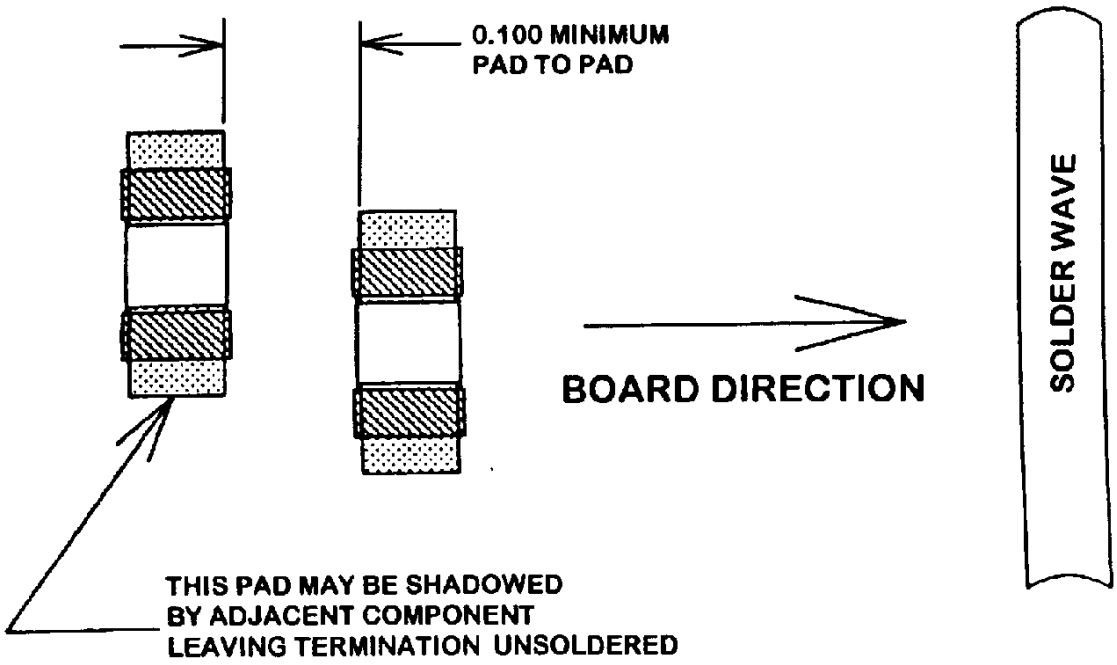


Figure 5-2 MINIMUM DISTANCE REQUIRED BETWEEN STAGGERED CHIP COMPONENTS WHEN WAVE SOLDERING

Minimum component spacing for the most common package types are shown in Figures 5-3 and 5-4. Care should be taken when designing with new or non-standard parts to provide the clearance required for assembly, rework and test. Generally the component to component spacing will be 1X the component height (preferred) or 1/2 the component height (minimum). Manufacturing engineering or the assembly vendor should be consulted when questions of spacing arise.

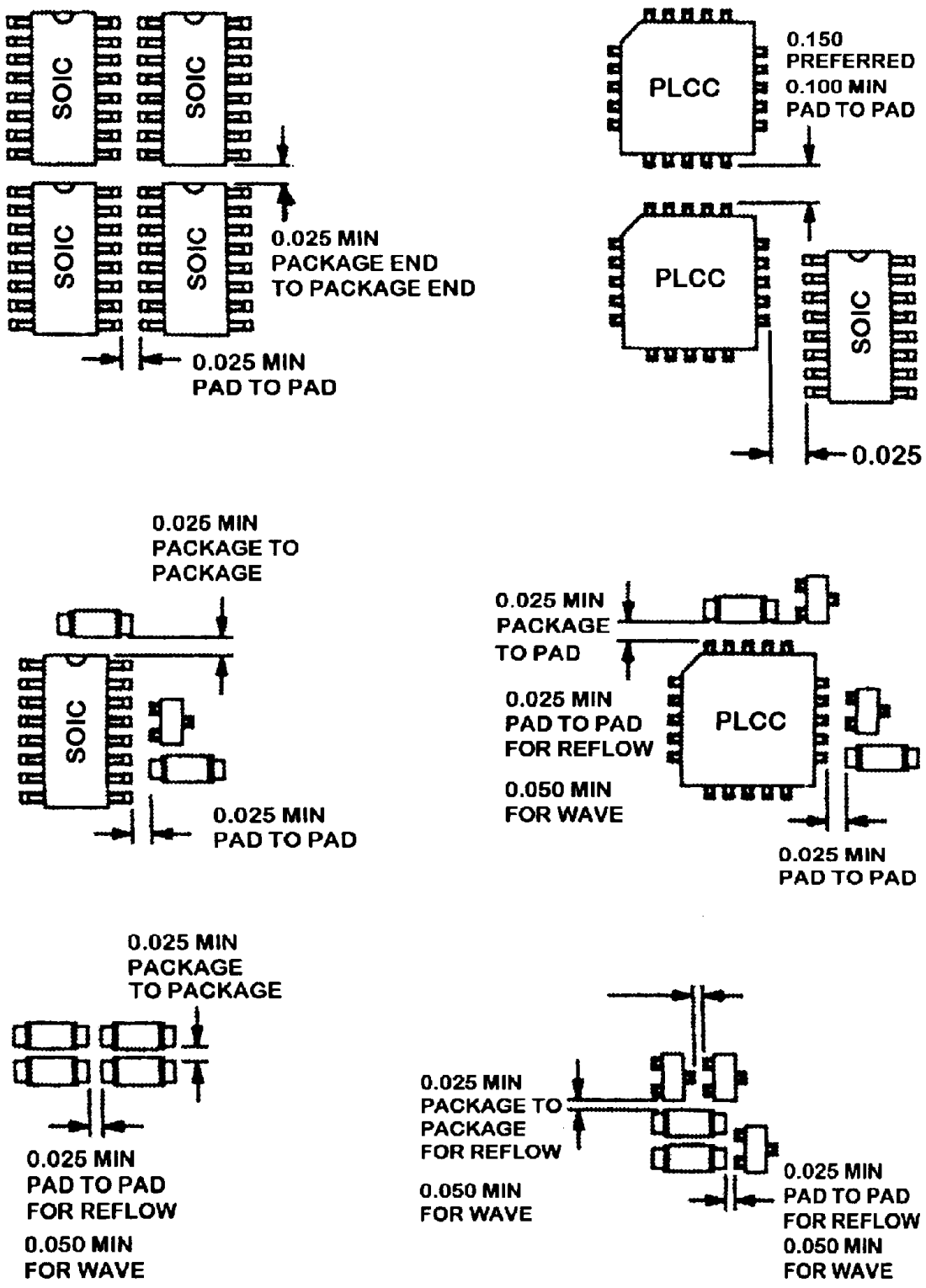


Figure 5-3 SMT COMPONENT SPACING

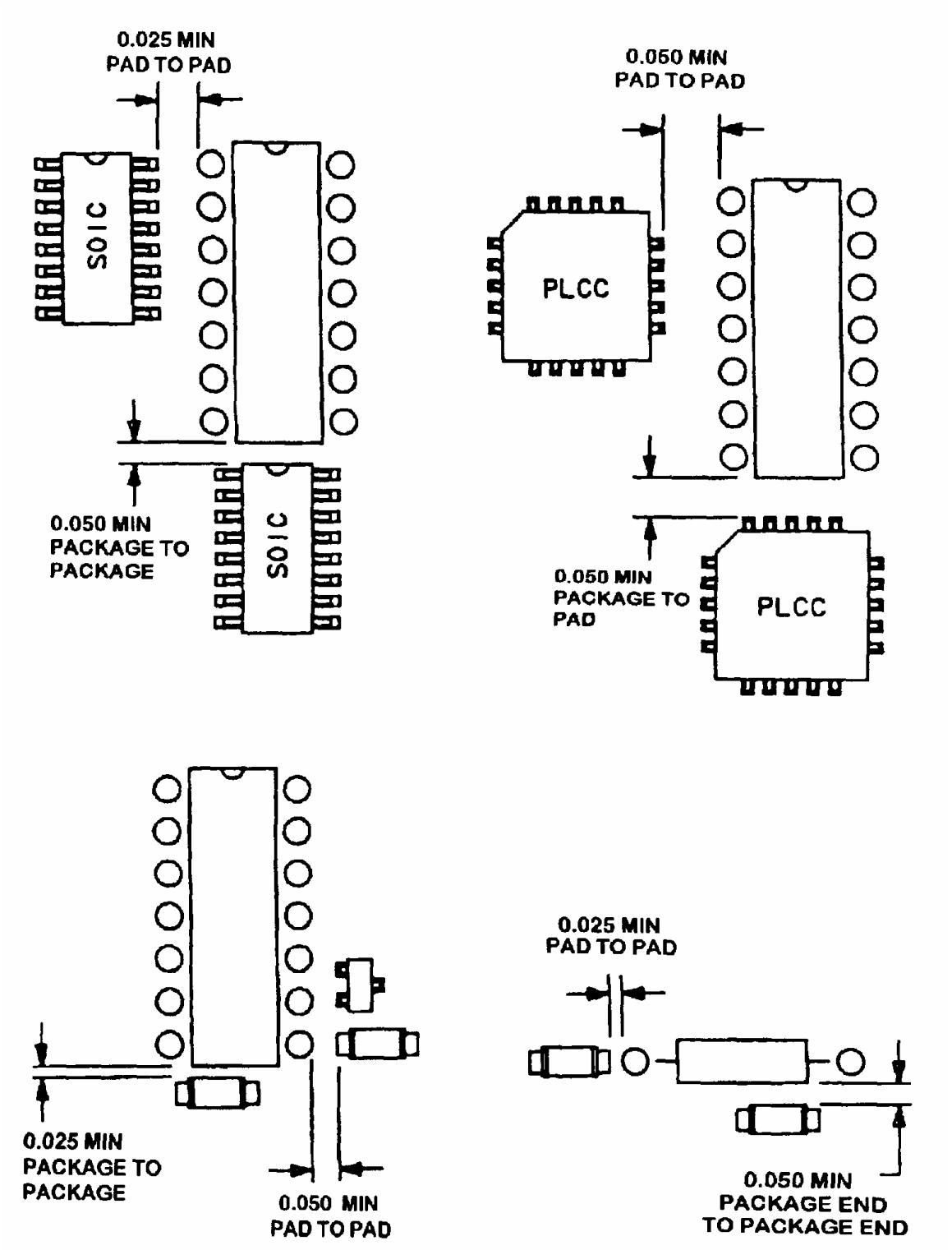
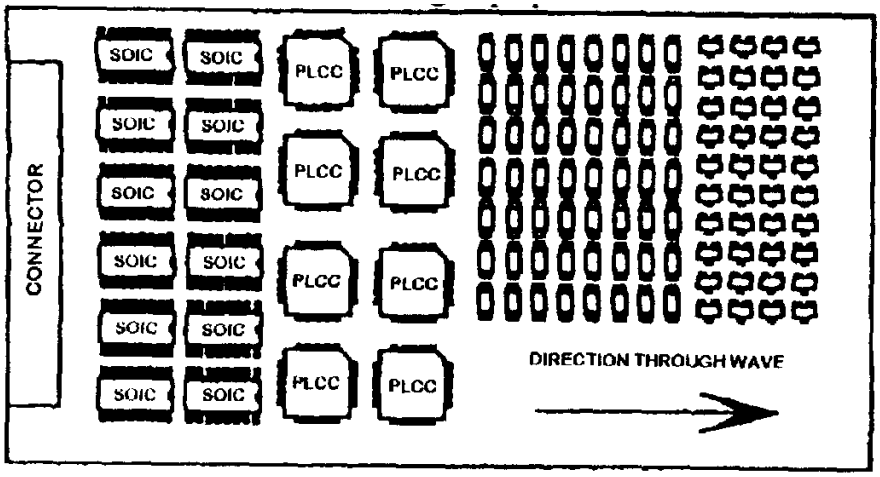


Figure 5-3 SMT TO THRU-PIN COMPONENT SPACING

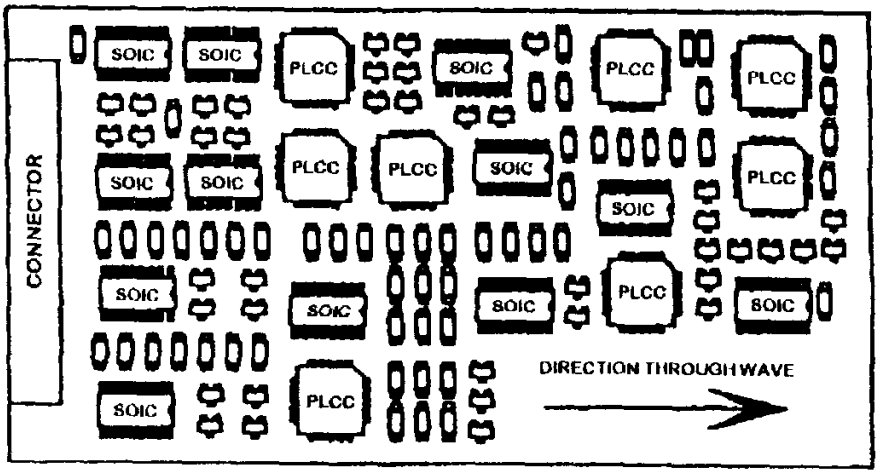
5.5 COMPONENT AND BOARD ORIENTATION

Component orientation has a direct effect on the quality and reliability of reflow and wave soldered assemblies. Poor unreliable solder joints, unsoldered connections and tombstoning (see Figure 5-6) of components are some results of incorrect placement and orientation. The size and geometry of the board outline, tooling holes, the location of connectors and components *at* the edge of a board will determine the direction of flow through placement and soldering equipment.



WHEN THE LARGE COMPONENTS ARE BUNCHED UP AS IN THIS DESIGN THE BOARD WILL HAVE TO BE REFLOWED AT HIGHER TEMPERATURES THAN NECESSARY AND DAMAGE TO CHIP COMPONENTS MAY OCCUR.

NON-PREFERRED COMPONENT PLACEMENT



BY SPREADING OUT THE LARGE COMPONENTS EVENLY OVER THE DESIGN, BETTER THERMAL DISTRIBUTION IS ACHIEVED FOR SOLDERING

Figure 5-5 PLACEMENT FOR THERMAL DISTRIBUTION

A component to component spacing equal to the height of the package should be used when designing with large components (over 0.20" high) such as SMT sockets, inductors and tantalum capacitors. This allows enough room for visual inspection and rework of solder joints.

Thermal considerations require that the component density be distributed about the available board space as evenly as possible and concentrations of large components be avoided. When components are spread out over the board, one area of the board will not be substantially hotter than another during reflow (see Figure 5-5). Even component distribution is also required to aid in balancing the routing across the surfaces and layers of the board and to minimize bow and twist. (See Section 6 for balanced routing requirements.)

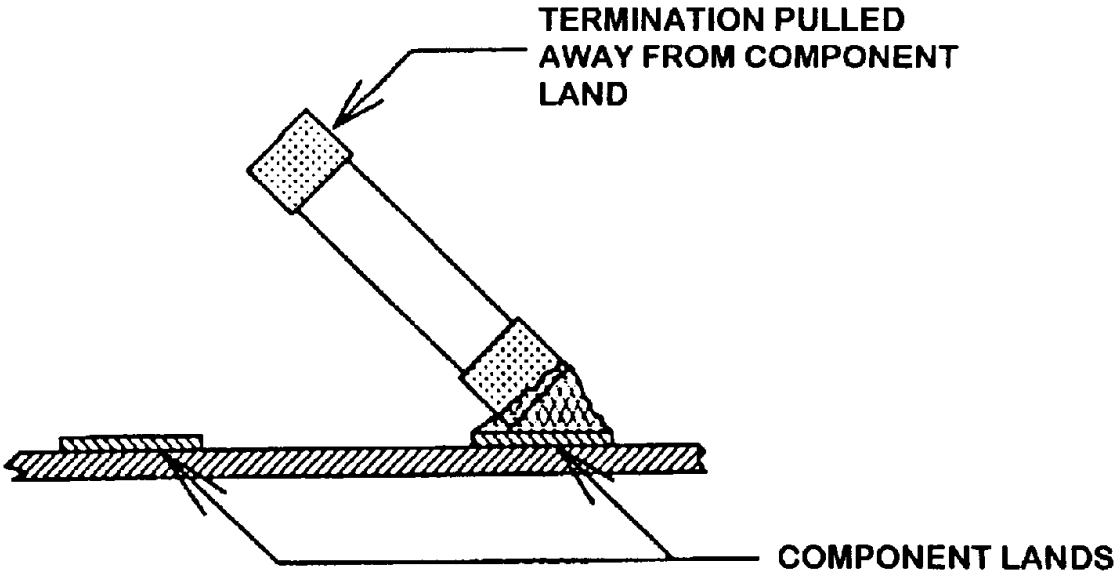


Figure 5-6 TOMBSTONED COMPONENT

5.6 BOARD ORIENTATION FOR WAVE SOLDER

It is desirable for the long axis of the board to be the direction of flow through the solder machine. This minimizes the building of fixtures to prevent sagging of the assembly when soldering. As an example, shown in Figure 5-7, the board of 9.50" x 12.00" must be soldered with the PCB traveling in the short axis, which is the non-preferred direction. This is because the card edge connectors interfere with gripping the assembly in the long axis. Extra time and tooling may be necessary to solder the assembly.

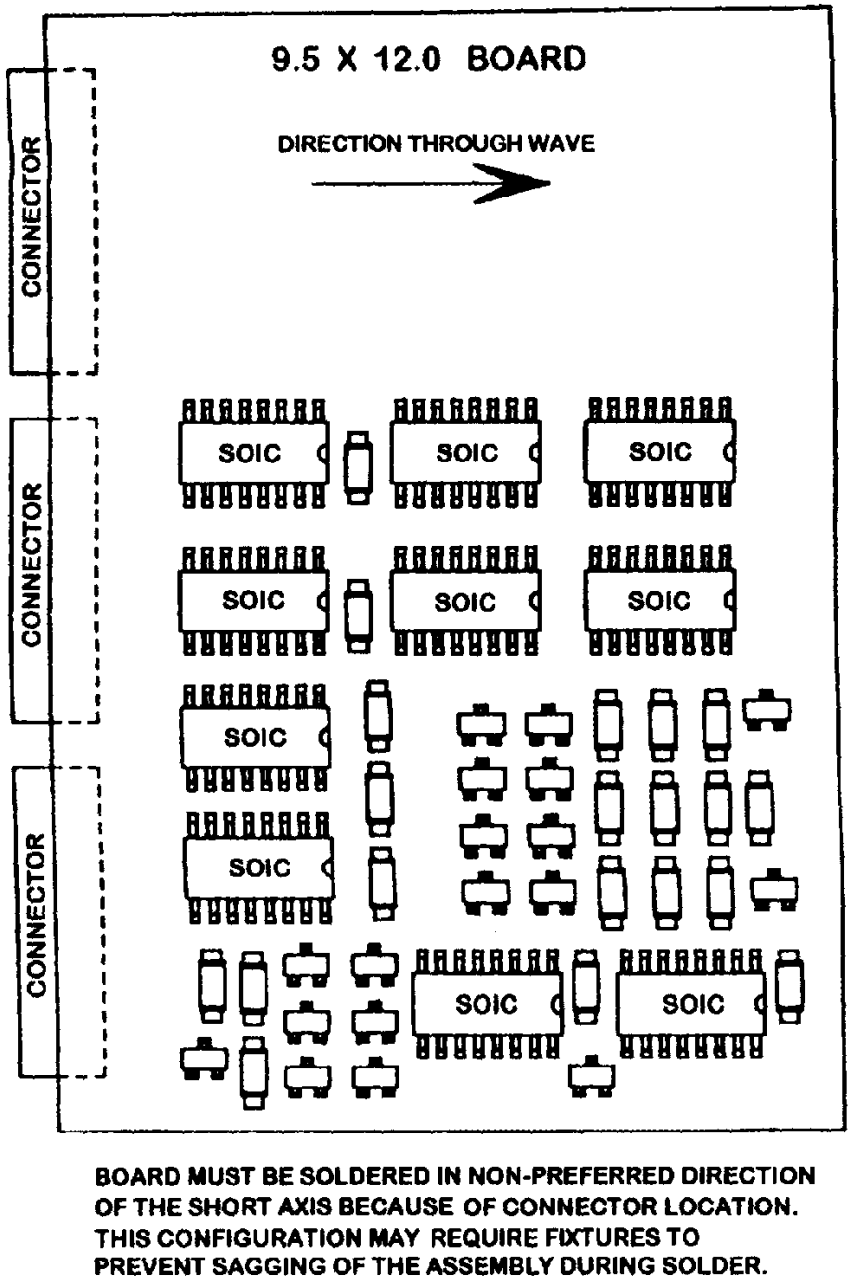
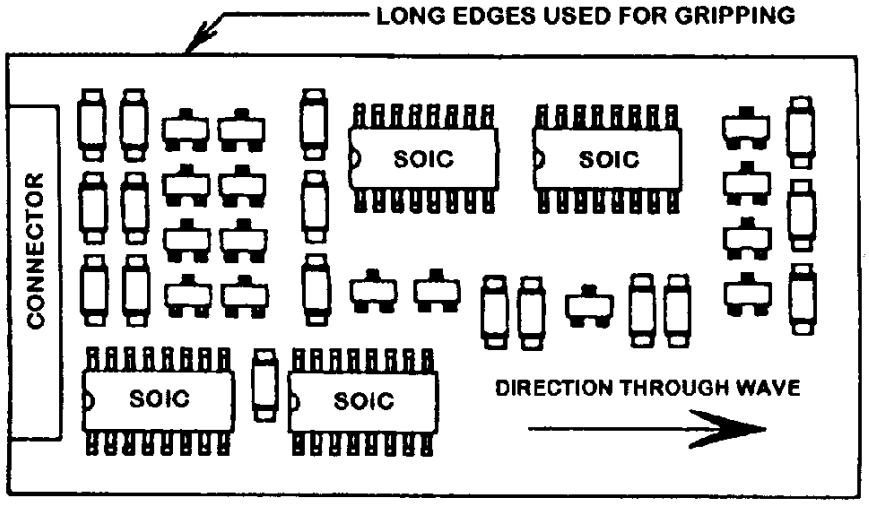


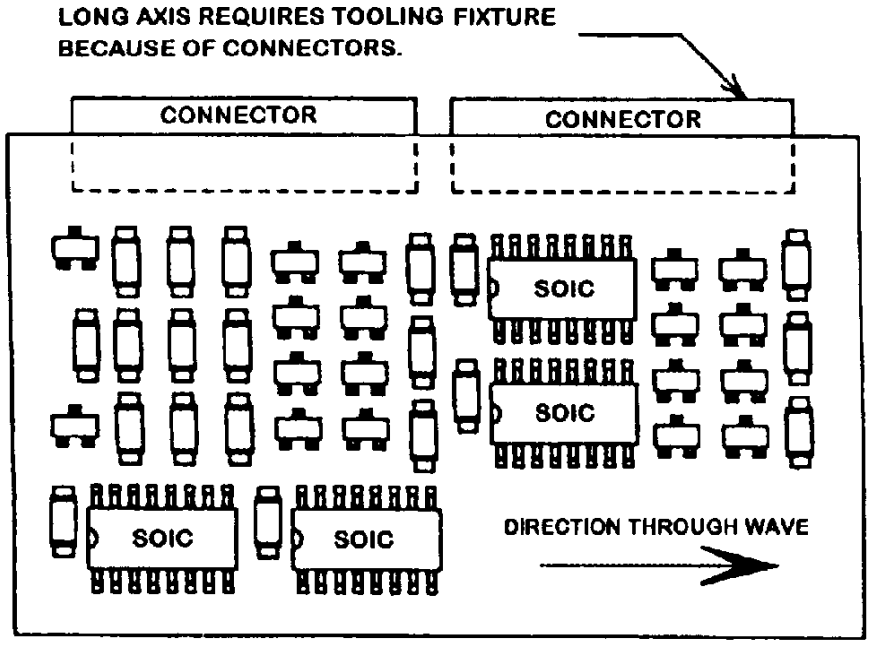
Figure 5-7 NON-PREFERRED BOARD TO SOLDER ORIENTATION

5.7 COMPONENT ORIENTATION

The preferred component orientation in relation to board outline and solder process is with the long axis of the PCB and SOICs parallel to the direction of flow through the solder equipment (see Figure 5-8).



PREFERRED ORIENTATION FOR TOP AND BOTTOM COMPONENTS.
BOARD IS SOLDERED IN THE DIRECTION OF THE LONG AXIS.



NON-PREFERRED

BOTTOM SIDE COMPONENT ORIENTATION FOR WAVE SOLDER. BOARD MAY REQUIRE A FIXTURE BECAUSE OF CONNECTOR LOCATIONS.

Figure 5-8 COMPONENT ORIENTATION

Chip components should be oriented parallel to the solder wave to insure the soldering of both terminations simultaneously. Avoid designs that place chips perpendicular to each other, which may result in shadowing, solder skips and uneven fillets. Uneven solder fillets will create excess stress on solder joints possibly causing the components to crack.

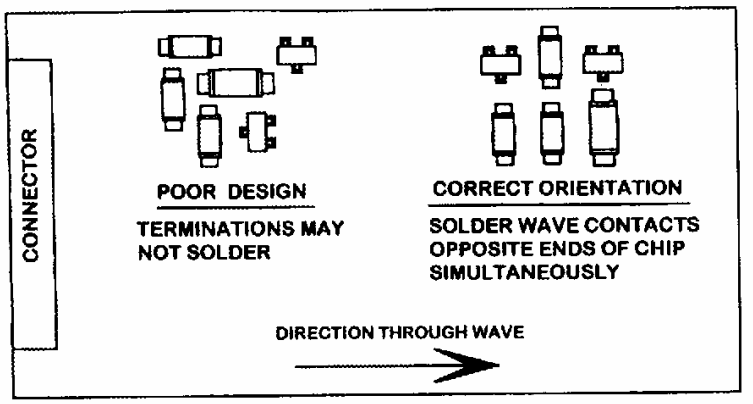


Figure 5-9 CHIP ORIENTATION

Placement which may cause smaller components to be shadowed from the solder wave should be avoided. This causes a high probability of creating open solder joints. The soldering direction of the board should be determined so that components such as tantalum caps and IC's will not shadow the solder wave from the smaller chip components (see Figure 5-10).

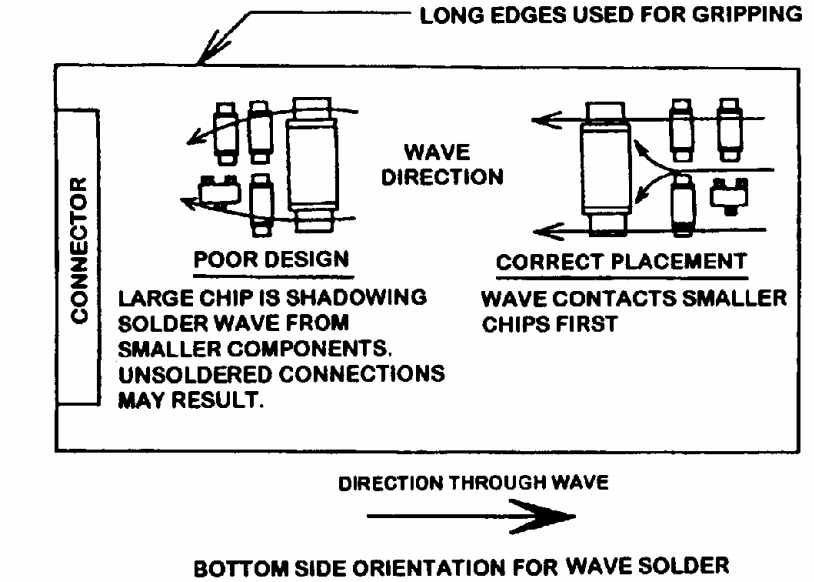


Figure 5-10 COMPONENT SHADOWING

5.8 CAPACITOR PLACEMENT

As an aid to assembly, all polarized capacitors will be placed with the positive end to the right or down. The polarity will be indicated on the silkscreen by a plus or other indicator (i.e. bar) on the package outline.

Chip decoupling capacitors on the top or bottom of the board will be placed perpendicular to SOICs and the solder flow. They will be placed as close as practical to the power pin of the IC.

5.9 COMPONENTS NOT RECOMMENDED FOR BOTTOM PLACEMENT

Some types of components are sensitive to the higher temperatures of wave soldering and should not be used on the bottom of boards where the solder wave would contact the component. Other types of components may not be suited to wave solder because of their lead configurations and size. The following is a list of components to avoid placing on the bottom of a board to be wave soldered:

Large body chip caps, package types 1812 and 1825 may crack when exposed to wave solder.

Memory and static ram chips which may be damaged by high temperatures.

The 1206 should be the smallest package size used on the solder side of the board. Smaller packages such as the 0805 are not well suited for epoxy application and wave solder.

PLCCs as the lead configuration is not suited to wave solder.

SOTs do not solder well due to leads being too close to component body.

SECTION 6: TRACE ROUTING

6.1 TRACE ROUTING TO COMPONENT LANDS

Large traces connecting to a component land may cause heat to migrate away from the component termination resulting in poor solder joints. In cases where solder mask is not used, solder may flow away from the component termination causing an open solder joint. Necking the trace down as it enters the land prevents the solder and heat from migrating away from the pad and helps to thermally balance the land pattern. The trace should be a maximum of 0.010" wide connecting to the pad and a minimum of 0.010" long from the pad to a large trace as shown in Figure 6-1. If the circuit design requires a wide trace to be connected to component lands, the traces connecting both lands should be the same width and the smallest possible dimension.

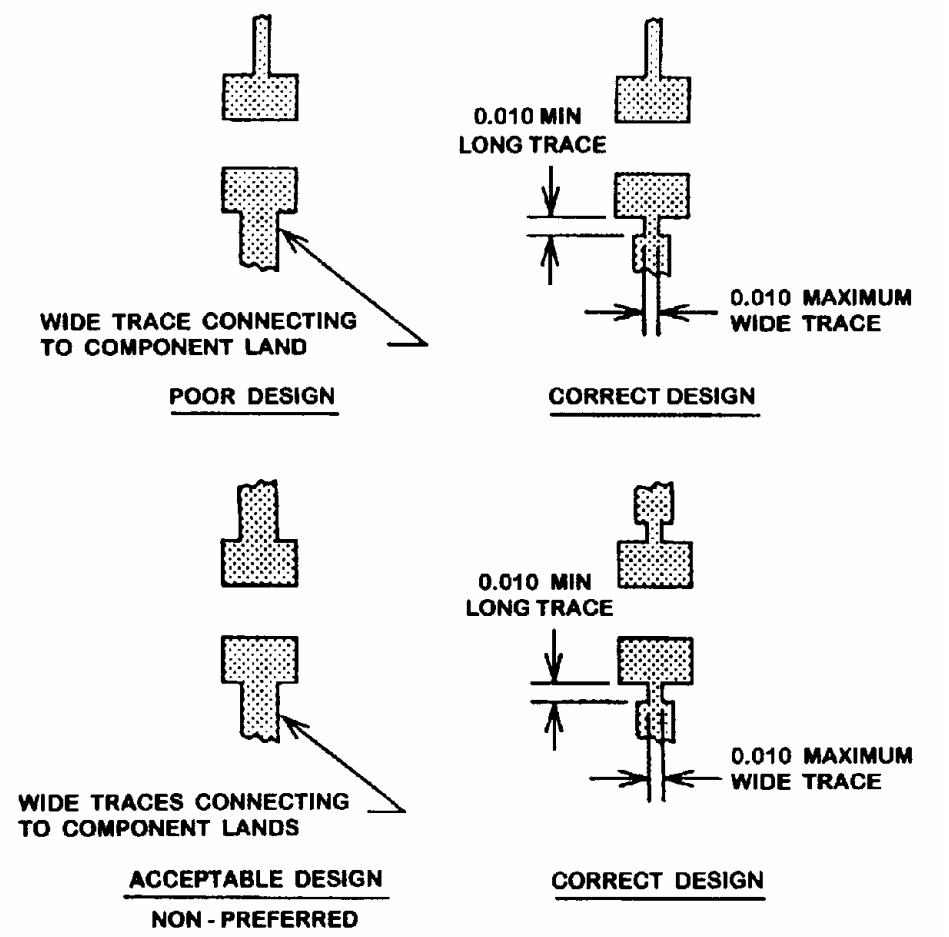


Figure 6-1 CONNECTING THICK TRACES TO COMPONENT LANDS

When connecting component pads to large ground traces, or wide high current conductors, the traces must be necked down and balanced to prevent the migration of heat (and solder if solder mask is not used) to large conductor areas. More than one trace may be used to connect ground planes and large traces to land patterns. The traces should be a maximum of 0.010" wide connecting to the pad and a minimum of 0.010" long from pad to large trace or plane (see Figure 6-2).

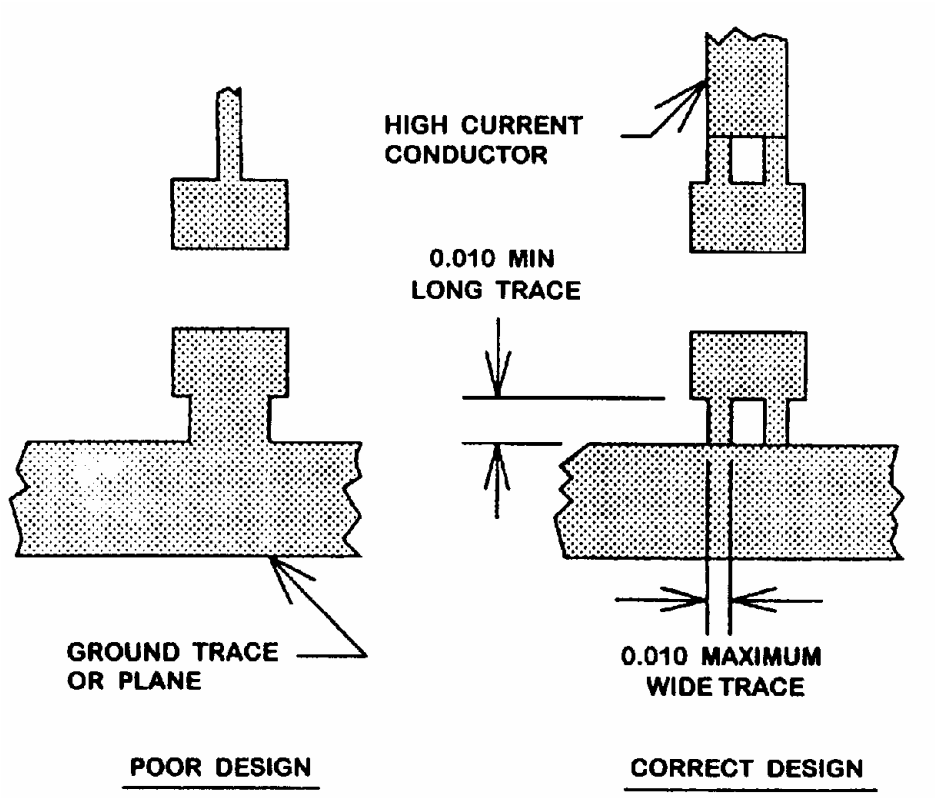


Figure 6-2 CONNECTING COMPONENT LANDS TO LARGE CONDUCTORS

Signal traces should connect to component pads using one trace per pad, preferably connecting to the outside or inside edges of the pads in a symmetrical manner. When using solder mask on the board, the angle and location of the connecting traces are not as critical as non-solder masked designs. Generally any routing which keeps the amount of trace connecting the component pads balanced will be acceptable. See Figure 6-3 for an example of trace routing.

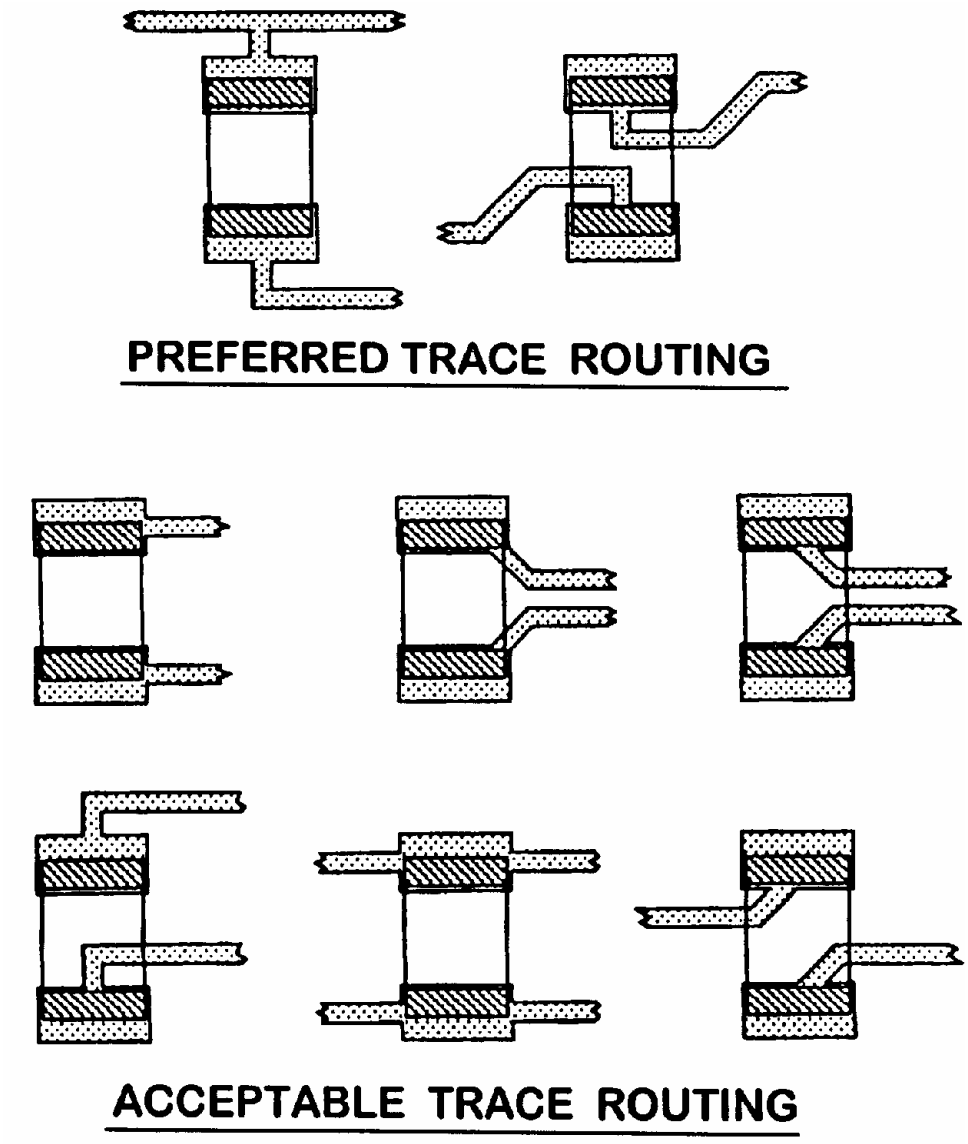


Figure 6-3 CONNECTING TRACES TO COMPONENT LANDS WHEN USING SOLDERMASK

When routing traces to chip component pads and solder mask is not used on the board, it becomes critical to route the connections in such a way to keep the solder from migrating away from the pad and pulling the component out of alignment. Traces should be routed to both inside or outside edges of the pad to keep the solder tension evenly distributed on both terminations of the component. Figure 6-4 shows the preferred method of connecting traces to chip pads.

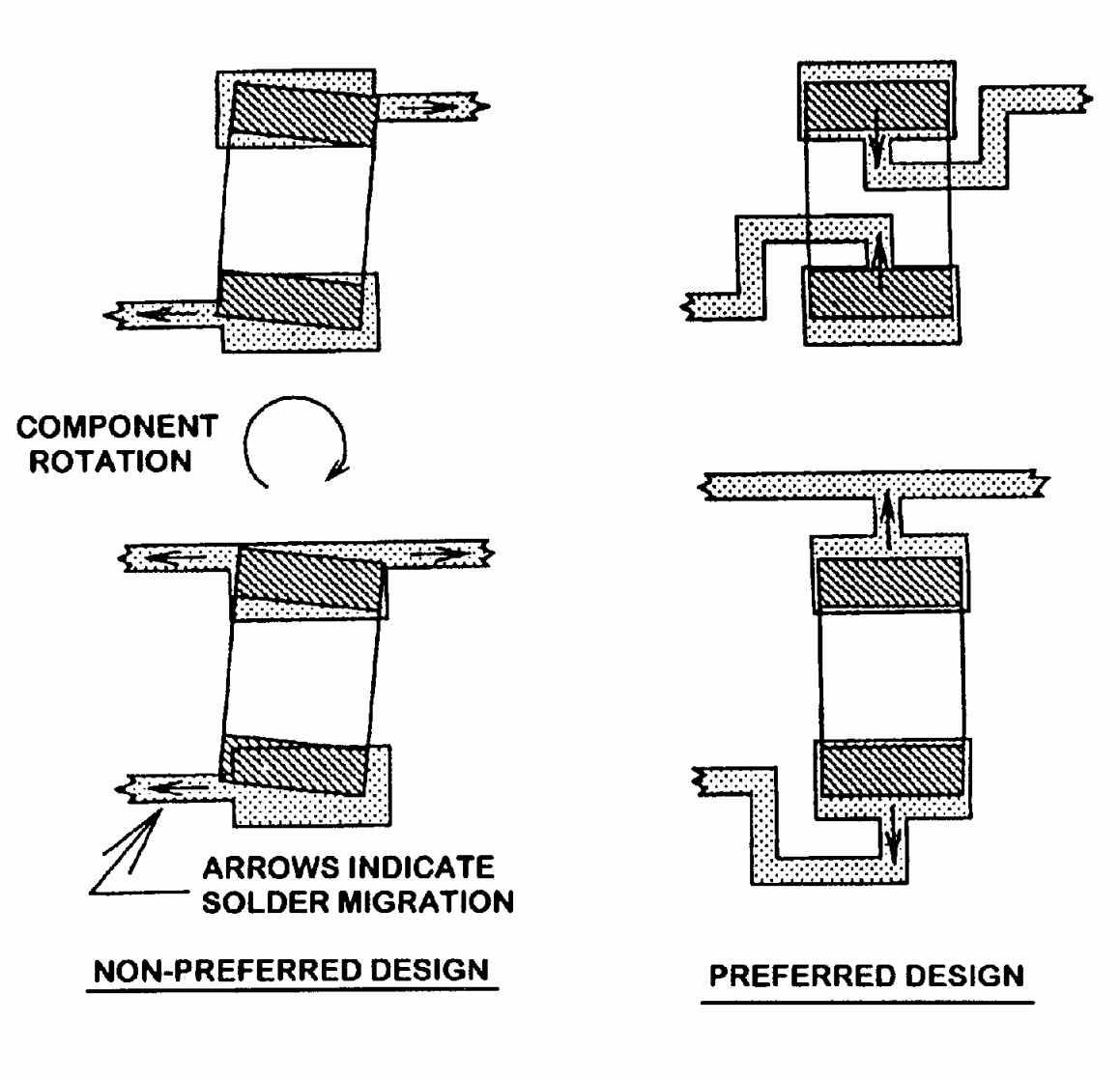


Figure 6-4 CONNECTING TRACES TO COMPONENT LANDS WHEN SOLDER MASK IS NOT USED

6.2 VIA ROUTING GUIDELINES

Test via spacing will be 0.100" preferred, 0.050" acceptable. Refer to Section 7 regarding test requirements for other pad to pad spacing requirements.

Do not place vias under axial through hole components as the component may be damaged during soldering when solder flows up through the via hole.

Do not place vias in a location where it would be possible to insert a component incorrectly. For example: 0.100" away from each end of a sip package.

The placing of vias under chip components on wave soldered assemblies is not recommended, as solder flowing up through the via may lift or break the component, or possibly short a component to pad. If the chip component is located on the solder side of the board, avoid placing vias under or near the component where it may interfere with areas used to epoxy the component to the board (see Figure 6-5).

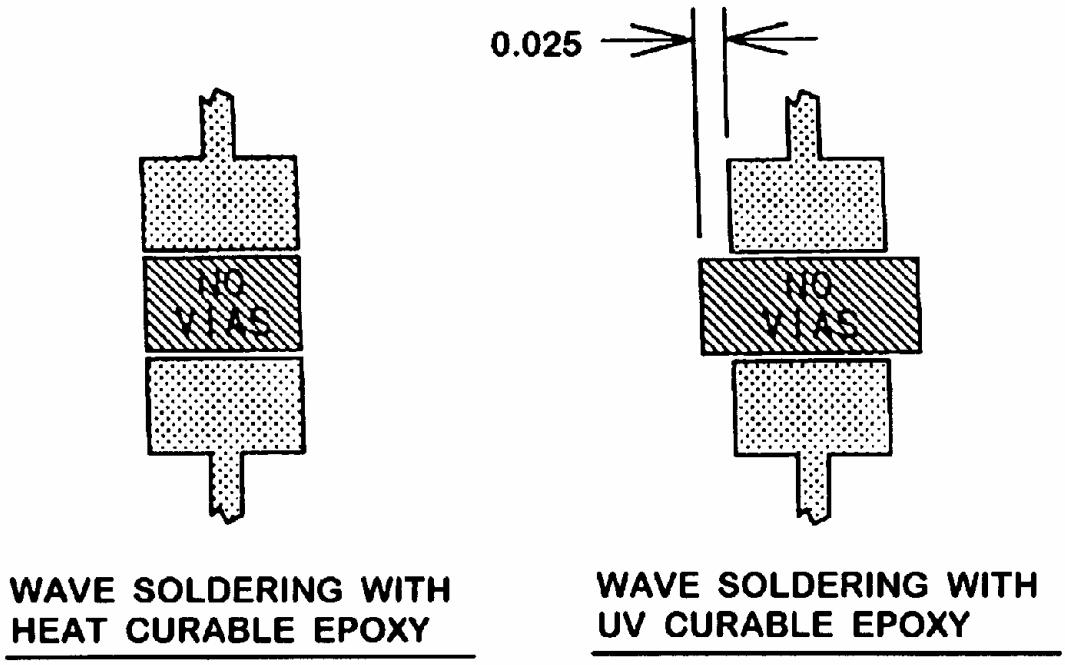


Figure 6-5 VIA PLACEMENT FOR SOLDER SIDE CHIPS

Vias connecting to a component pad shall have a minimum clearance of 0.010" from via edge to component land edge and maximum trace width of 0.010" (see Figure 6-6). Spacings under 0.010" are not recommended but may be useful on extra dense designs. If vias are to be placed closer than 0.010" to a component pad, they must be covered with solder mask.

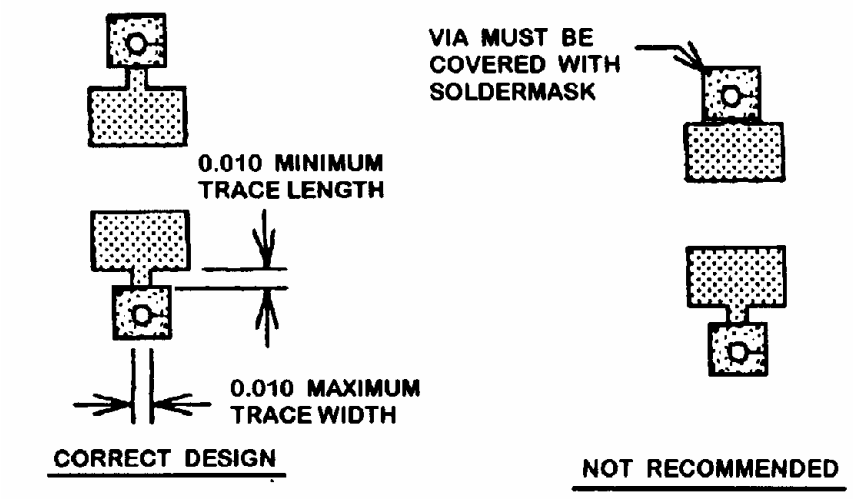


Figure 6-6 CONNECTING VIAS TO COMPONENT PADS

Vias not connecting to component pads will have a minimum clearance of 0.025". When the PCB is to be wave soldered, via clearance to component pads on the solder side of the PCB will be 0.040" if the via is placed before or after the pad in the direction of solder wave (see Figure 6-7).

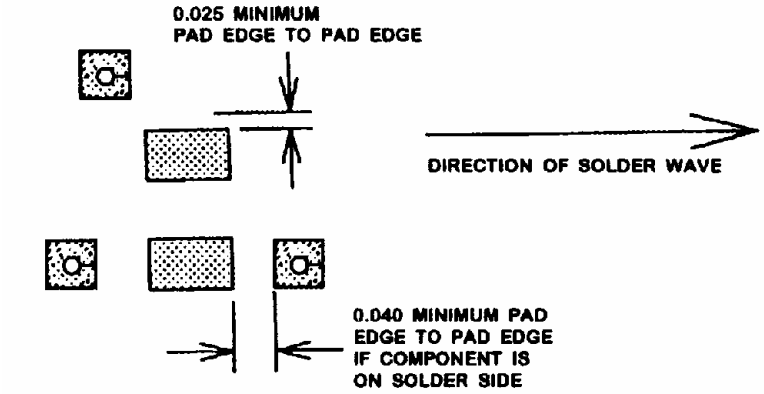


Figure 6-7 VIA TO COMPONENT PAD SPACING

SECTION 7: TEST REQUIREMENTS

7.1 GENERAL REQUIREMENTS

A minimum of one, but preferably two, test probe points per node (line or path on a schematic and all the component pins connecting to them) is required.

Components or component leads should never be used as test probe points. The test probe holding the component against the component land may cause a successful test of a cracked solder joint.

Avoid heavy concentrations of test probes in any one area as this may cause vacuum sealing problems, harmful flexing of the assembly and contact problems.

Provide access to all probe points from one side of the board. The solder side of the board is preferred as it will have zero or few components to interfere with probe locations. Access can be made from both sides of the board, but will result in a higher fixturing cost.

7.2 TEST PADS

Test probe pads may consist of vias, PTH component pads or remote test pads. A remote test pad may be a specific test point with a terminal installed at that location (i.e. TP1, TP8) or a one sided pad (no through hole) on the side of the board to be accessed by the test probes (see Figure 7-1).

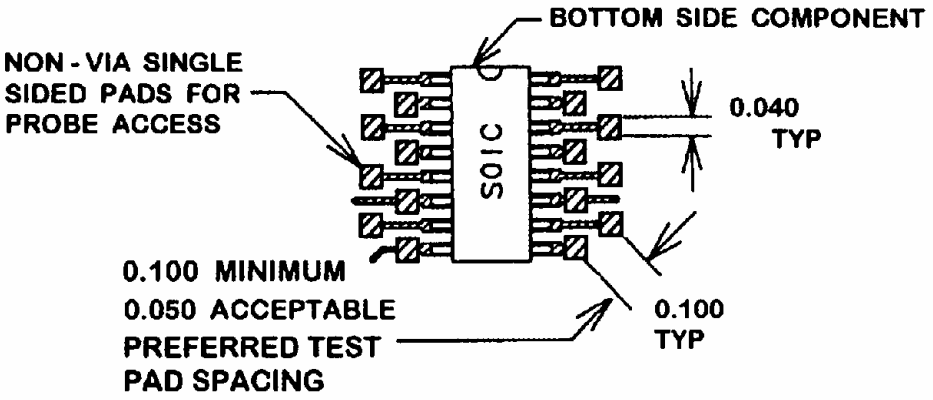


Figure 7-1 NON-THROUGH HOLE TEST PADS

A minimum pad size of 0.035" will be used for test probe points. A minimum pad size of 0.040" is recommended when a board size exceeds 12 inches in either dimension. Smaller pad sizes may be used but generally increase the cost of fixturing and testing of the assembly.

Probe pads should not be placed within 0.125" of the board edge.

7.3 TEST PAD SPACING

Test probe pads will be a minimum of 0.100" apart, pad center to pad center, to allow for use of the large more reliable probes. Spacings closer than 0.100" are possible, but when pad spacing falls below 0.100", smaller, less reliable and more costly probes must be used (see Figure 7-2). Pad center to pad center should be no closer than 0.050".

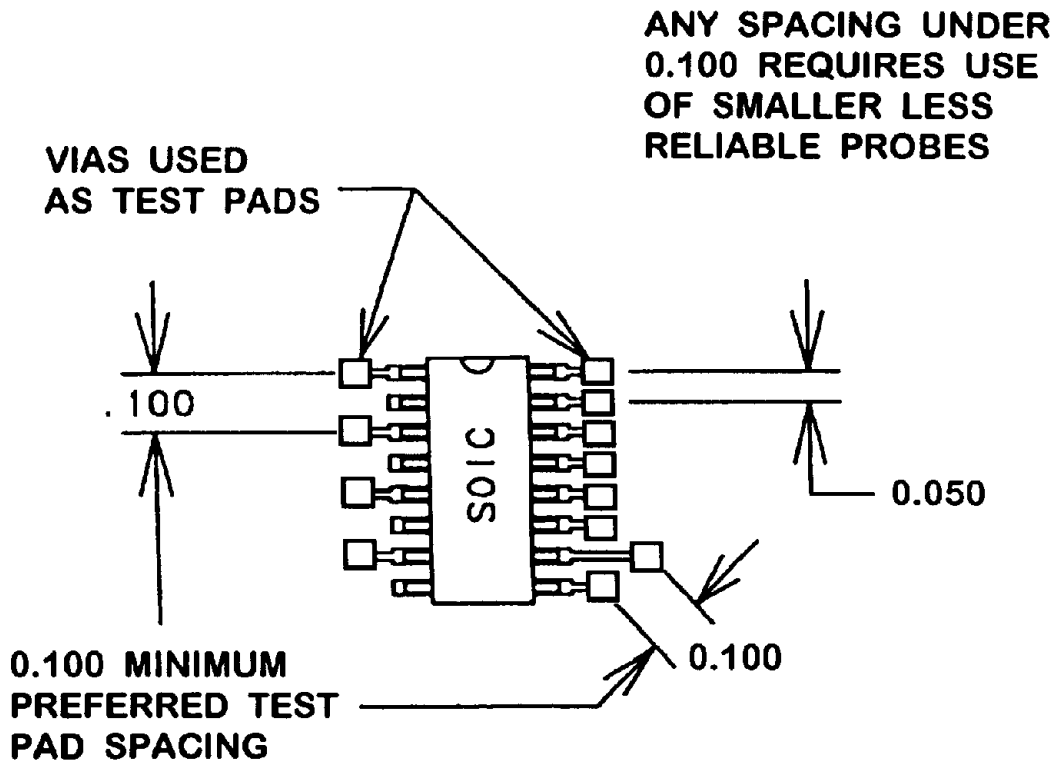


Figure 7-2 TEST PAD SPACING

Test pad centerlines must be located a minimum of 0.200" from the edge of components over 0.200" high (see Figure 7-3). If the pad to component spacing falls below the minimum, the test probe may be located in the milled out clearance area for the component. This can result in reduced support and mounting complications for the probe.

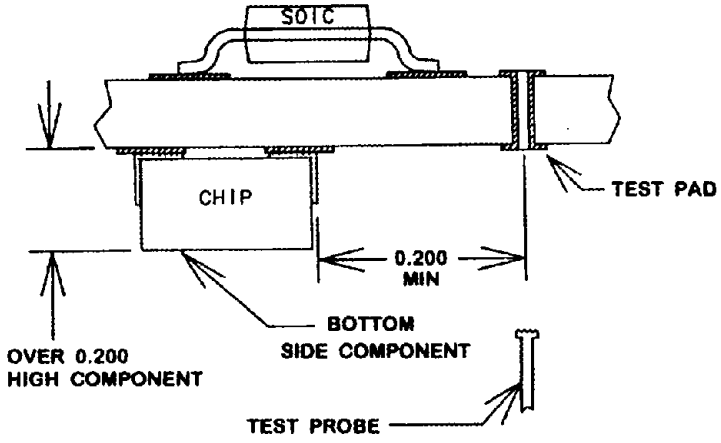


Figure 7-3 TEST PAD TO COMPONENT SPACING (COMPONENTS OVER 0.200" HIGH)

Test pads near components less than 0.200" high should be placed such that the centerline of the pad is located 0.060" minimum away from the body of the component. This is to prevent probe damage caused by a probe inadvertently hitting a component because of tolerances in fixturing and component placement (see Figure 7-4).

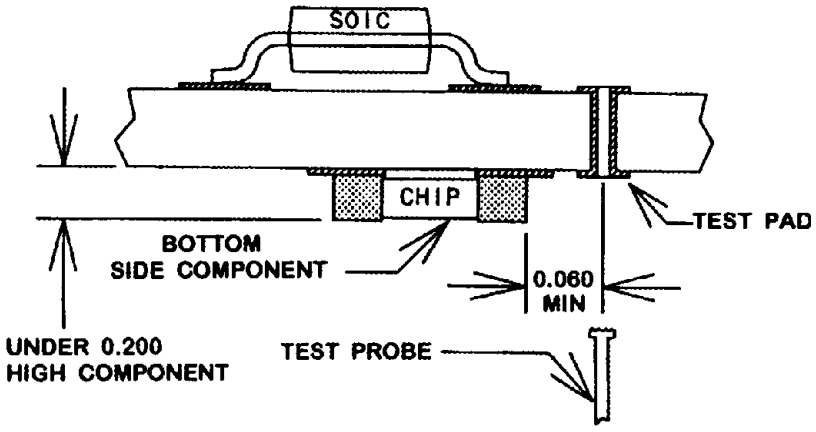


Figure 7-4 TEST PAD TO COMPONENT SPACING (COMPONENTS UNDER .200" HIGH)

7.4 COMPONENT PLACEMENT

Components should not be placed within 0.150" (0.250" preferred) of the edge of the board to provide a free area for vacuum sealing and grasping of the board.

7.5 TEST TOOLING REQUIREMENTS

Provide two tooling holes of 0.125" diameter with a tolerance of + 0.002". The holes must be diagonally opposite each other and include a component free area of 0.125" annular radius. Tooling hole to probe pad (circuit image) tolerance should be + 0.002".

SECTION 8: STENCIL REQUIREMENTS

8.1 GENERAL STENCIL REQUIREMENTS

The solder paste artwork layer is used to create a stencil for the application of solder paste to the PCB before surface mount components are placed on the board. This artwork may be in the form of a 1:1 photoplot or gerber file and aperture list. The film will contain board targets, film labels and all the surface mount pads to which solder paste will be applied. The surface mount template pads on the pastemask film are to be identical in size and pattern to the surface mount pads in the circuit layers. NO EXPANSION IS REQUIRED.

Manufacturing or the assembly vendor may or may not have a need to modify the film to meet the requirements of the solder process. When an assembly contains only surface mount components to be mounted on both sides of the board, and the board is to be reflow soldered only, both component and solder side stencil artwork is required. The layers of film are to be labeled "SOLDER STENCIL (COMPONENT SIDE)". Solder stencil film must be generated with the emulsion side up and right reading.

SECTION 9: THROUGH HOLE AUTO INSERTION

9.1 BOARD GUIDELINES

The following is a list of board dimensions for auto inserting through hole:

Maximum Board Thickness: 0.090"
Maximum Board Size: 18" X 18"
Tooling Holes: Should be on the same edge of the board, 0.500" away from components, must not be plated, and 0.125" in diameter
Drilling: Boards should not be stacked more than 3 high when drilling

9.2 AXIAL COMPONENTS

Minimum Hole Diameter: 0.035" and 0.015" greater than lead diameter
Maximum Lead Diameter: 0.036"
Maximum Body Diameter: 0.265"
Minimum Hole Spacing: 0.050" greater than component body
Center to Center Spacing: 0.300" to 0.800"

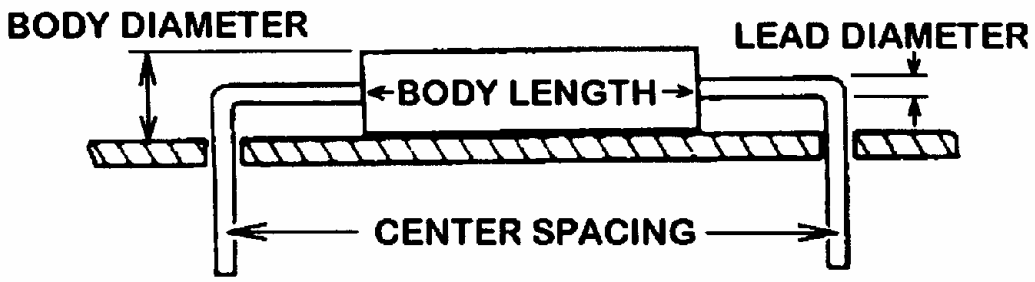


Figure 9-2 AXIAL COMPONENT

9.3 DIP COMPONENTS

Prepping: DIPs must NOT be prepped
Spacing: Must be spaced 0.100" apart from side to side
Maximum Pin Count: 40 pin maximum on DIPs

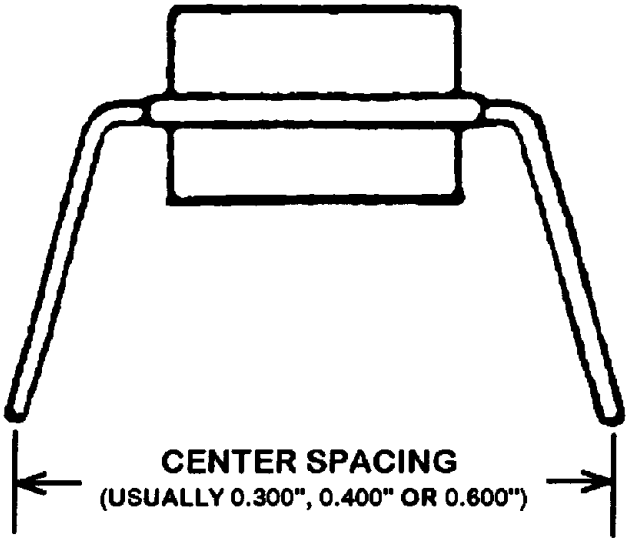


Figure 9-3 SIDE VIEW OF A DIP COMPONENT

SECTION 10: AUTOMATED OPTICAL INSPECTION

10.1 COMPUTER INTEGRATED MANUFACTURING

Altron utilizes Computer Integrated Manufacturing, which enables us to improve our responsiveness to initial project setup as well as engineering changes. This software system allows us to convert your CAD design data and bill of material data into a wide array of useful information more quickly and accurately than possible with manual methods.

In order to successfully process your assemblies using computer integrated manufacturing, we will require a bill of materials and one of the following groups of board design data. However, if more information and formats are available, please provide them since they can be beneficial in coping with any unforeseen file difficulties.

10.2 BILL OF MATERIALS

Preferred Format: Capable of handling most formats, but prefer:

1. Excel Spreadsheet with at least reference and part numbers.
2. ASCII text file with at least reference and part numbers.
3. Delimiters do not affect ability to import.
4. Example: R1-65, R98, 105, 108-200 10000-901 Resistor 2K R0603

The bill of materials is essential to processing the assembly. If you are not familiar with the above formats or if you know you cannot obtain a bill of materials in electronic form, please contact our sales department to discuss other options.

10.3 Board Design Data

Fortunately all CAD systems output Gerber data, therefore you can be assured that at least this data has been available at some time in the product's life cycle. The photoplotters used to fabricate bare boards are driven by this data exclusively and therefore, if a bare board exists, someone had access to the Gerber data at one time.

At least one of the sets of data listed below will be required. (The sets are listed in order of preference, 1 being most preferred.):

Set 1: Native CAD File Import Format

Altron will provide guidance to customers regarding extracting the needed native data from their board design software.

Set 2: Gerber Data Files

Set 3: ASCII Centroid File

The centroid list or file is used to program the pick and place machines. This is a listing of the exact center of every component and fiducial mark on the printed circuit board. Most CAD systems will export this file and it is sometimes referred to as an "insertion file", "manufacturing file", or "CAM file". It can also be used as a sole source of CAD information but this is not desirable since these files lack graphical information required for good visual aid and documentation development. Table 10-1 shows an example of the centroid and data required.

Assembly #: 123-456
Revision: A
Component Side (or Solder Side)

Reference Designator	X Coordinate	Y Coordinate	∅ Orientation	Part Number
U1	123.30	23.45	0	ABC-123
U3	37.62	14.25	180	DEF-456
C1	12.3	85.77	90	GHI-789

Table 10-1 Example Of Centroid Data

SECTION 11: DEFINITIONS

BGA (BALL GRID ARRAY) - A surface mount component typically made of either plastic or ceramic. These parts are characterized by the lack of pins, instead they have balls of solder as their means of conduction to the board. The solder balls are made up of either Sn63Pb37 or Snl0Pb90. The advantage of BGAs over conventional quad flat packs is their ability to exceed the lead count limitations per area of quad flat packs.

CHIP - The uncased and normally leadless form of an electronic component, either passive or active, discrete or integrated. Chip components have metallized terminations for interconnecting to the solder pad. The case type number of a chip component indicates its size. For example: a 1206 chip is 0.120" long by 0.060" wide, and a 1812 chip is 0.180" long by 0.120" wide.

COMPONENT SIDE (TOP) - A term used to describe the component loaded side of a PWB using through hole technology.

CONDUCTOR - An electrical path between two component pads. Also referred to as a **“**trace”, “path”, or “line”.

CTE (COEFFICIENT OF THERMAL EXPANSION) - The linear thermal expansion per unit change in temperature.

FIDUCIAL MARK - A round pad or other mark on the surface of a PWB used for optically aligning automatic insertion equipment to the component footprints on the board.

GULL WING LEAD - A lead configuration typically used on small outline integrated circuits (SOIC). The package and formed leads, when viewed together from the end, resembles a gull in flight.

J-LEAD - A lead configuration typically used on plastic leaded chip carriers (PLCC). The lead is rolled under the component body causing formed lead to resemble the letter "J" when viewed from the side.

LAND ("PAD") - A portion of a conductive pattern used for attachment or connection of components.

LAND PATTERN ("LANDS" OR "PADS") – A combination of lands intended for the mounting and interconnection of a particular component.

MELF (METAL ELECTRODE LEADLESS FACE) - A cylindrical component package having metallization on both ends. This type of package is commonly used for diodes, capacitors and resistors.

NOMINAL - The measurement about which the tolerance is given. Halfway between minimum and maximum dimensions.

NSMD (NON SOLDER MASK DEFINED PAD) - A pad design characterized by the opening in the solder mask being larger than the copper pad for a BGA.

PAD - See LAND

PTH (PLATED THROUGH HOLE) - A hole in which electrical connection is made between external or internal layers or both, by the plating of metal on the wall of the hole. Also used for mounting the leads of through hole components.

PLCC (PLASTIC LEADED CHIP CARRIER) - A square component package commonly having J-leads on all four sides.

PWB (PRINTED WIRING BOARD) - A substrate of epoxy glass and clad metal or other material upon which completely processed, printed wiring has been formed.

REFLOW SOLDER - A process of soldering surface mount components to a PWB by mass heating of the entire assembly. The heating process causes solder paste, preapplied to component land patterns, to melt and form solder fillets between the component leads and land patterns on the board. Two types of reflow soldering are used, infrared and vapor phase.

INFRARED REFLOW (IR) - The process of soldering a surface mount assembly by using radiant (focused) or convective (non-focused) heat to melt the solder paste and form the solder fillet.

VAPOR PHASE REFLOW (VP) - The process of soldering a surface mount assembly by using the latent heat of vaporization of an inert liquid to melt the solder paste.

SHADOWING - The shadowing of the solder wave from small components by larger components or through hole component pins.

SMD[1] (SURFACE MOUNT DEVICE) - A device that is not inserted into through holes, but designed for placement and soldering onto the surface of a substrate.

SMD[2] (SOLDER MASK DEFINED) - A pad design characterized by an overlap of the opening of the solder mask on a copper pad (for a BGA).

SMT (SURFACE MOUNT TECHNOLOGY) - The technology of assembling printed wiring boards and hybrid circuits where components are mounted onto the surface of the substrate rather than onto through holes.

SOIC (SWISS OUTLINE INTERGRATED CIRCUIT or SMALL OUTLINE INTEGRATED CIRCUIT - "SWISS" is the original definition) - An integrated circuit package having two parallel rows of gull wing leads. Packages currently range from 8 to 40 leads.

SOT (SMALL OUTLINE TRANSISTORS) - A discrete semiconductor package having two gull wing leads on one side and one on the other side.

SOLDER BRIDGING - The formation of a conductive path or "short" between conductors during soldering.

SOLDER FILLET - A general term used to describe the contour of the solder joints formed between the component termination and the PWB land pattern after soldering.

SOLDER MASK - A coating of material used to protect or mask conductive traces or areas of a PWB against solder bridging.

SOLDER PASTE - A combination of minute spherical solder particles, flux, solvent and a suspension agent which is used in reflow soldering. Solder paste is deposited onto the substrate by solder dispensing and screen or stencil printing.

SOLDER SIDE (BOTTOM) - A term used to describe the soldered side of a PWB using through hole technology.

TOMBSTONE (DRAWBRIDGE) - The condition which exists when a defect in soldering, component orientation, component type or other factors have caused one end of a chip component to pull off the solder pad resulting in a solder open. The component may stand on end in a vertical or near vertical position.

TOOLING HOLES - A general term used for holes or slots in PWBs or blank material to aid in the manufacturing process.

TRACE - A conductive path or line.

TYPE I PCB - All surface mount component technology with components mounted on one or both sides of the board. The assembly may be reflow soldered in one or two passes.

TYPE II PCB - Mixed component technology, with surface mount components mounted on one or both sides of the board and through hole components mounted on the component side (top) of the board. Component side surface mount components are reflow soldered on the first pass and the solder side (bottom) surface mount components and through hole components are wave soldered on the second pass.

TYPE III PCB - Mixed component technology, with through hole components mounted on the component side (top) of the board and surface mount components mounted on the solder side (bottom) of the board. The assembly can be wave soldered in one pass.

VIA - A plated through hole used as a through connection for conductors from the component side to solder side of the board or an outer layer to an inner layer**.** A via is not intended for mounting components.

BLIND VIA - A via which connects an outer layer to one or more inner layers but not to both outer layers.

BURIED VIA - A via which connects one or more inner layers, but not to an outer layer.

WAVE SOLDER - The soldering of an assembly by passing the surface mount components, mounted on the solder side of the board, over an adhesive and then over a molten wave of solder. Typically through hole components installed on the top side of the board are soldered at the same time. The application of solder paste is not required for this assembly.

SECTION 12: BIBLIOGRAPHY

1. The Institute for Interconnecting and Packaging Electronic Circuits (1996). ***IPC-A-610 Acceptability of Electronic Assemblies,*** Revision B, Northbrook, IL

2. Joint Industry Standard (1995). ***ANSI/J-STD-OO1A,*** Revision A.

3. Surface Mount Technology Association (January 1996). ***JOURNAL OF SURFACE MOUNT TECHNOLOGY,*** Volume 9, Issue 1.

NOTES